STM32Lx – 低功耗系列

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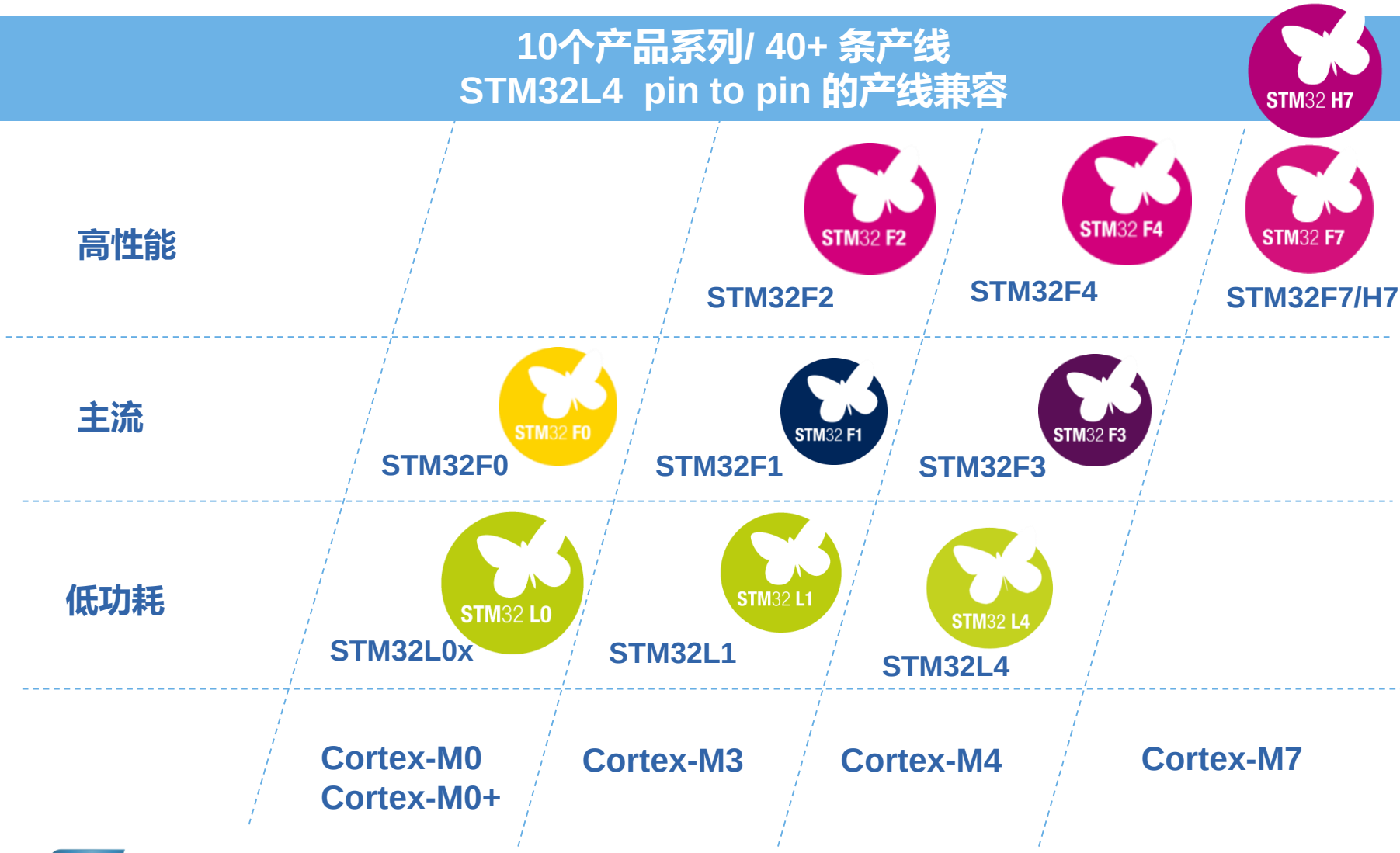
STM32 L4：STM32 L系列的新成员

10个产品系列/ 40+ 条产线
STM32L4 pin to pin 的产线兼容



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STM32L 超低功耗全系列

STM32L4 完善超低功耗系列

STM32 L0
超低功耗入门型

Cortex-M0+ @ 32 MHz
Operating range:
1.65 to 3.6V
8/16-bit applications
Numerous pin counts

3 product lines,
Cost-effective,
Smaller packages
USB, LCD, Analog
16 to 192 Kbytes of Flash
Up to 20 Kbytes of SRAM

STM32 L1
超低功耗

Cortex-M3 @ 32 MHz
Operating range:
1.65 to 3.6V
Wide choice of
memory sizes

3 product lines,
USB, LCD, AES,
Rich Analog
True EEPROM,
Dual bank Flash (RWW)
32 to 512 Kbytes of Flash
Up to 80 Kbytes of SRAM

超低功耗
兼顾高性能

Cortex-M4 w/ FPU @ 80 MHz
Operating range:
1.71 to 3.6V
Advanced Peripheral
Performance

3 product lines,
ADC 5 Msps, PGA,
Compar., DAC, op amp,
USB OTG, LCD, AES
128 Kbytes to 1 Mbyte of
Flash
Up to 128 Kbytes of SRAM

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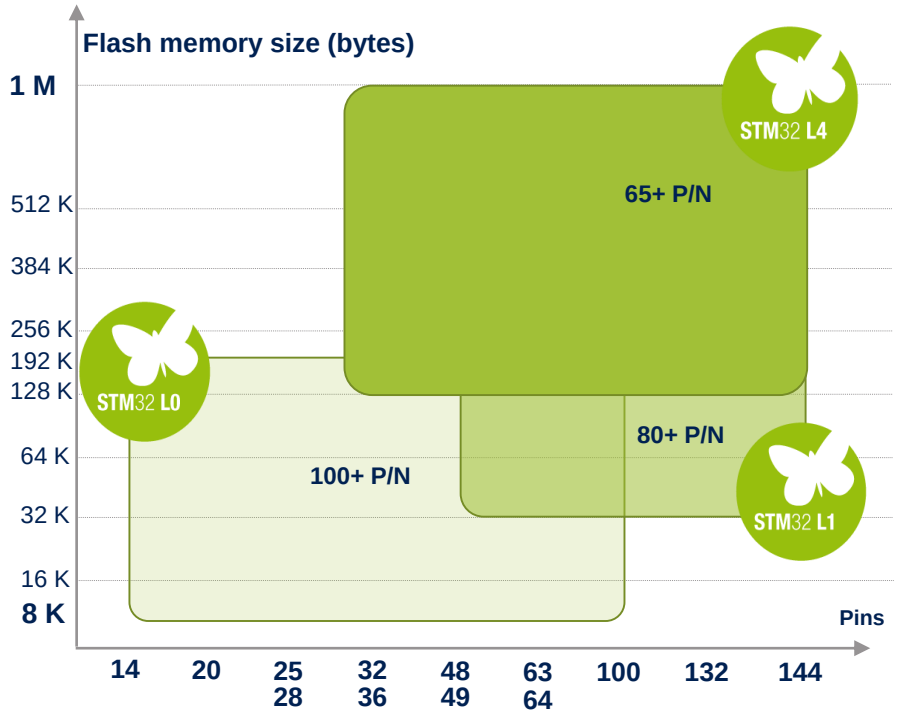
STM32Lx 全系列

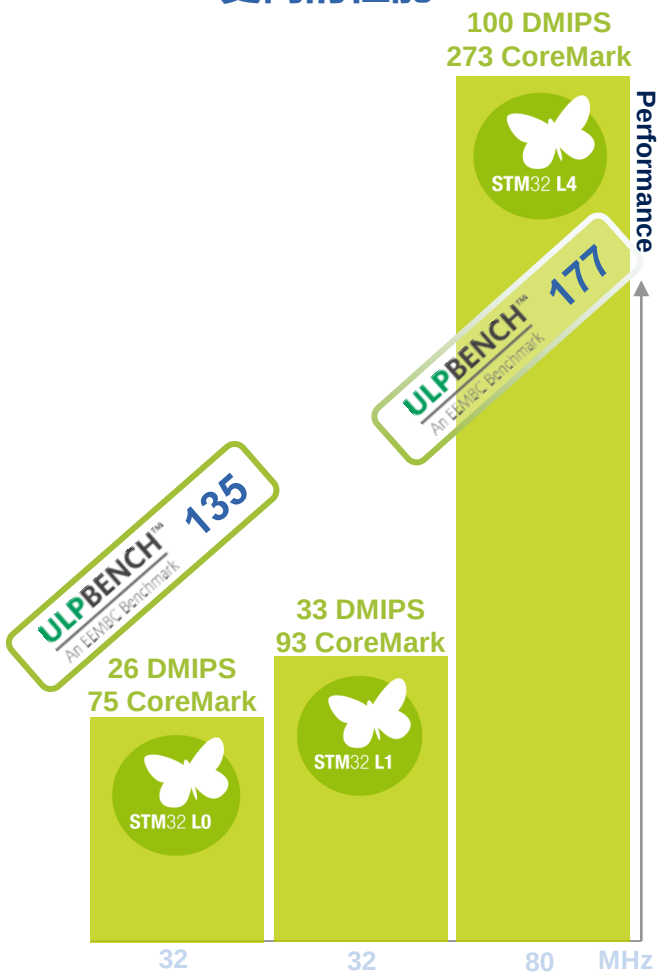
250 Part Numbers

更多的内存,功耗,外设和封装选择

更多的管脚和内存



更高的性能



更多种的封装

Packages

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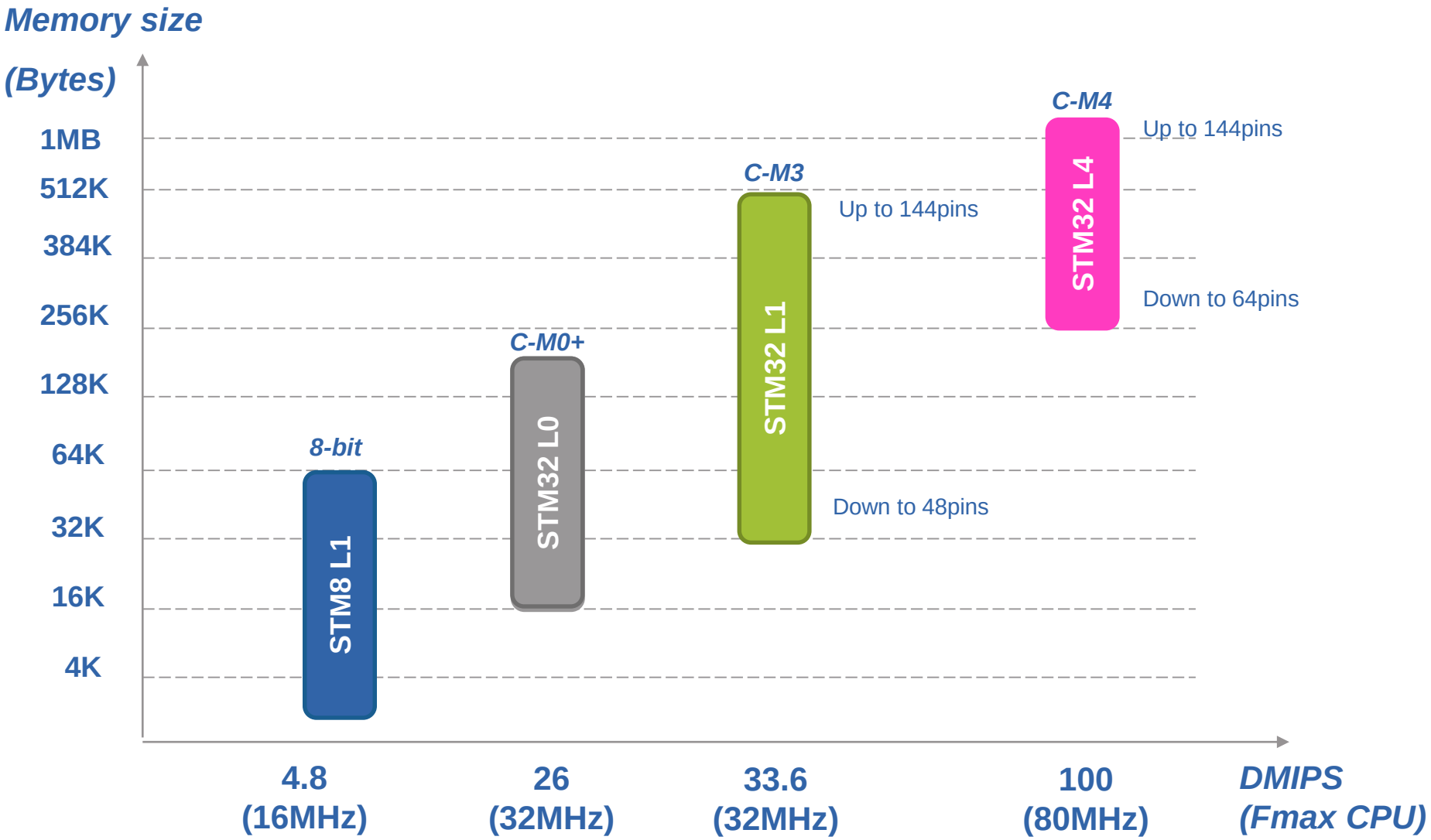
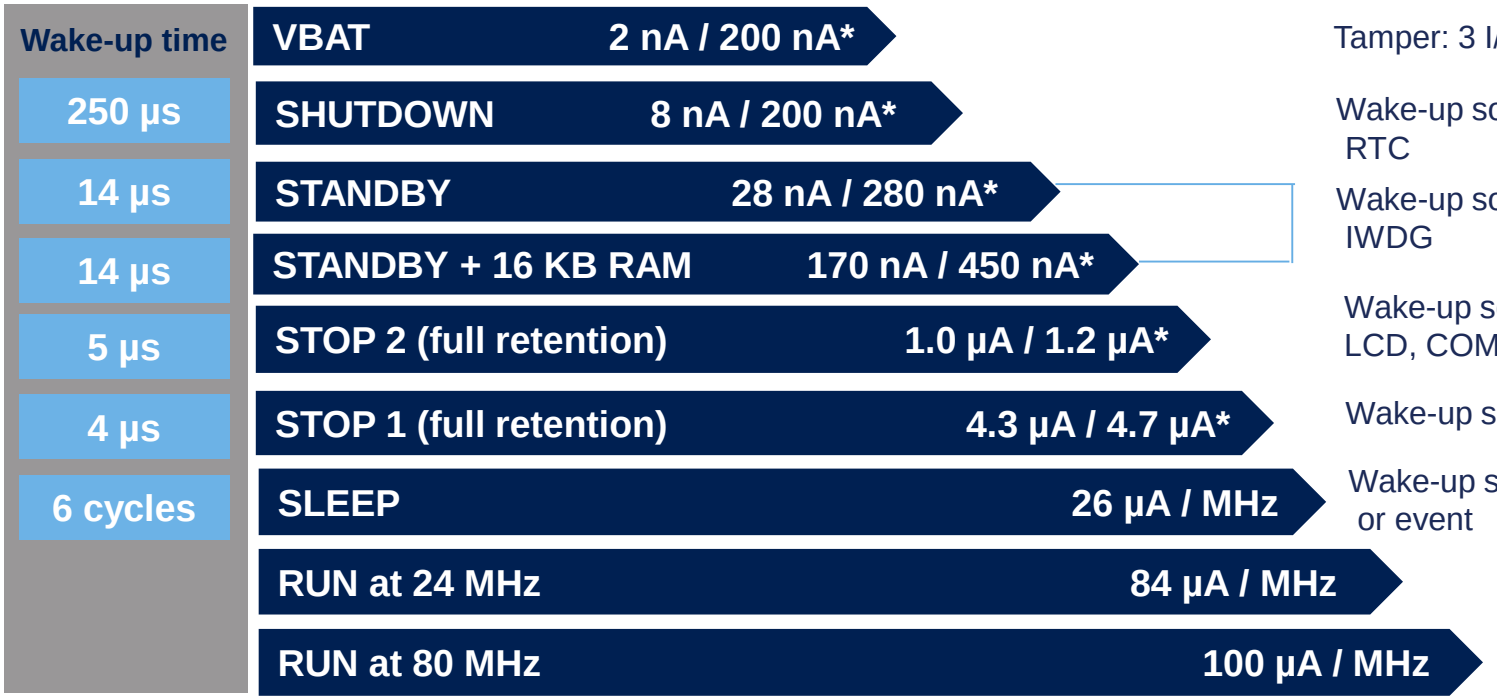
STMx 低功耗系列


Memory size
(Bytes)
1MB
512K
384K
256K
128K
64K
32K
16K
4K
8-bit
STM8 L1
C-M0+
STM32 L0
C-M3
STM32 L1
Up to 144pins
Down to 48pins
C-M4
STM32 L4
Up to 144pins
Down to 64pins
4.8
(16MHz)
26
(32MHz)
33.6
(32MHz)
100
(80MHz)
DMIPS
(Fmax CPU)

STM32L4的不同功耗模式

Best power consumption numbers with full flexibility



Tamper: 3 I/Os, RTC

Wake-up sources: reset pin, 5 I/Os, RTC

Wake-up sources: + BOR, IWDG

Wake-up sources: + all I/Os, PVD, LCD, COMPs, I²C, LPUART, LPTIM

Wake-up sources: + all I²C, UART

Wake-up sources: any interrupt or event

Note : * without RTC / with RTC

ULPBENCH™ 176.7
An EEMBC Benchmark

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High integration

High integration with high memory size in small packages

Parallel Interface
FSMC 8-/16-bit (TFT-LCD, SRAM, NOR, NAND)

Display
LCD driver 8 x 40

Timers
17 timers including:
2 x 16-bit advanced motor control timers
2 x ULP timers
7 x 16-bit-timers
2 x 32-bit timers

I/Os
Up to 114 I/Os
Touch-sensing controller

Cortex-M4
80 MHz
FPU
MPU
ETM

DMA

ART Accelerator™

Up to 1-Mbyte Flash with ECC Dual Bank

128-Kbyte RAM

Connectivity
USB OTG,
1x SD/SDIO/MMC, 3 x SPI, 3 x I²C, 1x CAN, 1 x Quad SPI,
5 x USART + 1 x ULP

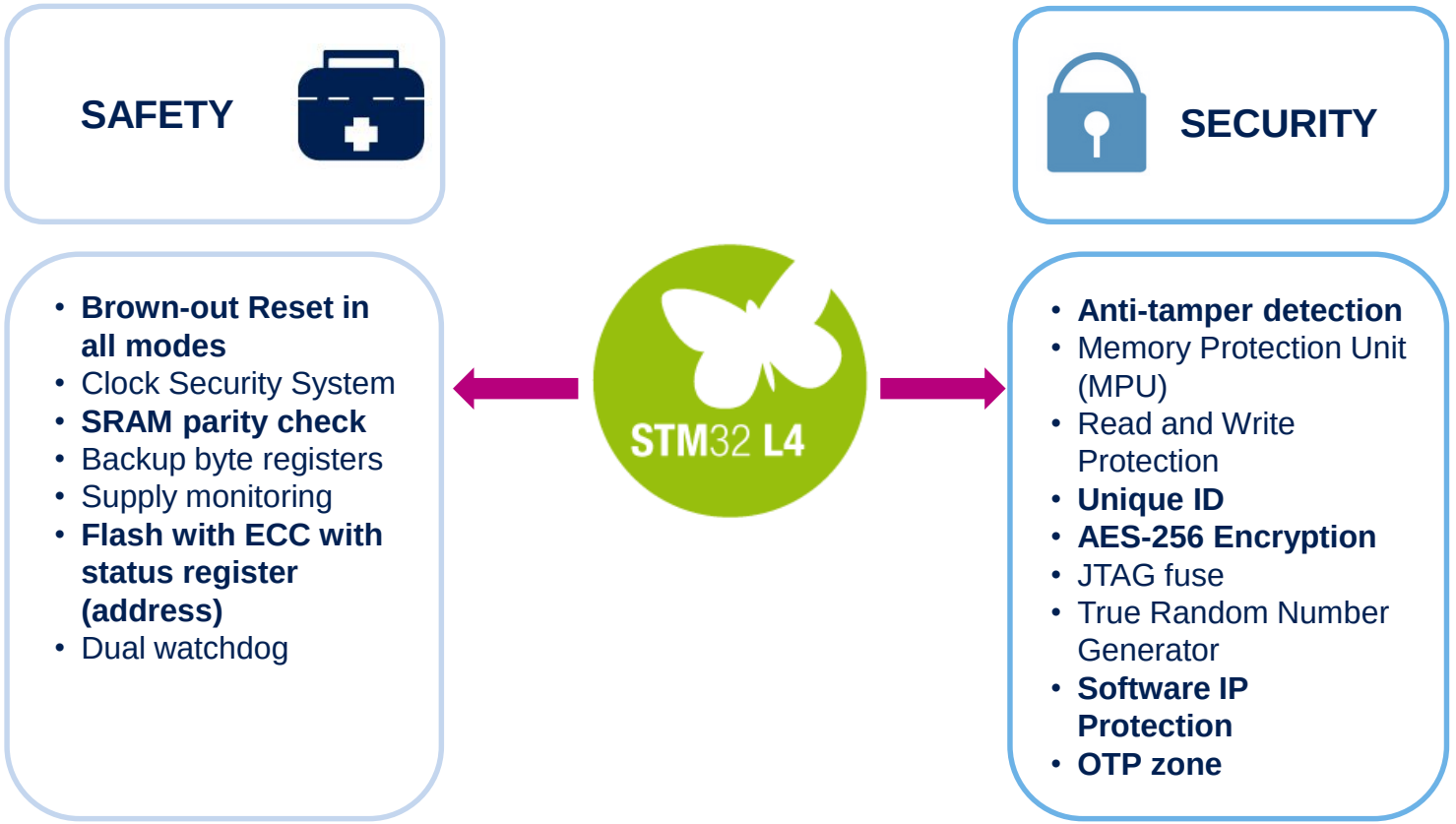
Digital
AES (256-bit), TRNG, 2 x SAI, DFSDM (8 channels)

Analog
3 x 16-bit ADC, 2 x DAC,
2 x comparators, 2 x op amps
1 x temperature sensor

Package size down to 3.13 x 3.14 mm

Safety and security

Integrated safety and security features



STM32L4 series

Cortex®-M4 (DSP + FPU) – 80 MHz

- ART Accelerator™
- USART, SPI, I²C
- QuadSPI
- 16 and 32-bit timers
- SAI + audio PLL
- SWP
- 1x CAN
- 2x 12-bit DAC
- Temperature sensor
- Low voltage 1.71V to 3.6V
- Vbat Mode
- Unique ID
- Capacitive Touch sensing
- TRNG

Product line	FLASH (KB)	RAM (KB)	Op-Amp	Comp	12- bit ADC 5 Msps 16 bit HW oversampling	USB2.0 FS Crystal-less	USB2.0 OTG FS	Segment LCD Driver	AES 128-256 bit
STM32L431 Access	Up to 256	64	x1	x2	x1				
STM32L432 USB FS	Up to 256	64	x1	x2	x1	●			
STM32L433 USB FS & LCD	Up to 256	64	x1	x2	x1	●		Up to 8x40	
STM32L443 USB FS & LCD & AES	256	64	x1	x2	x1	●		Up to 8x40	●
STM32L471 Access	Up to 1024	128	x2	x2	x3				
STM32L475 USB OTG	Up to 1024	128	x2	x2	x3		●		
STM32L476 USB OTG & LCD	Up to 1024	128	x2	x2	x3		●	Up to 8x40	
STM32L486 USB OTG & LCD & AES	1024	128	x2	x2	x3		●	Up to 8x40	●

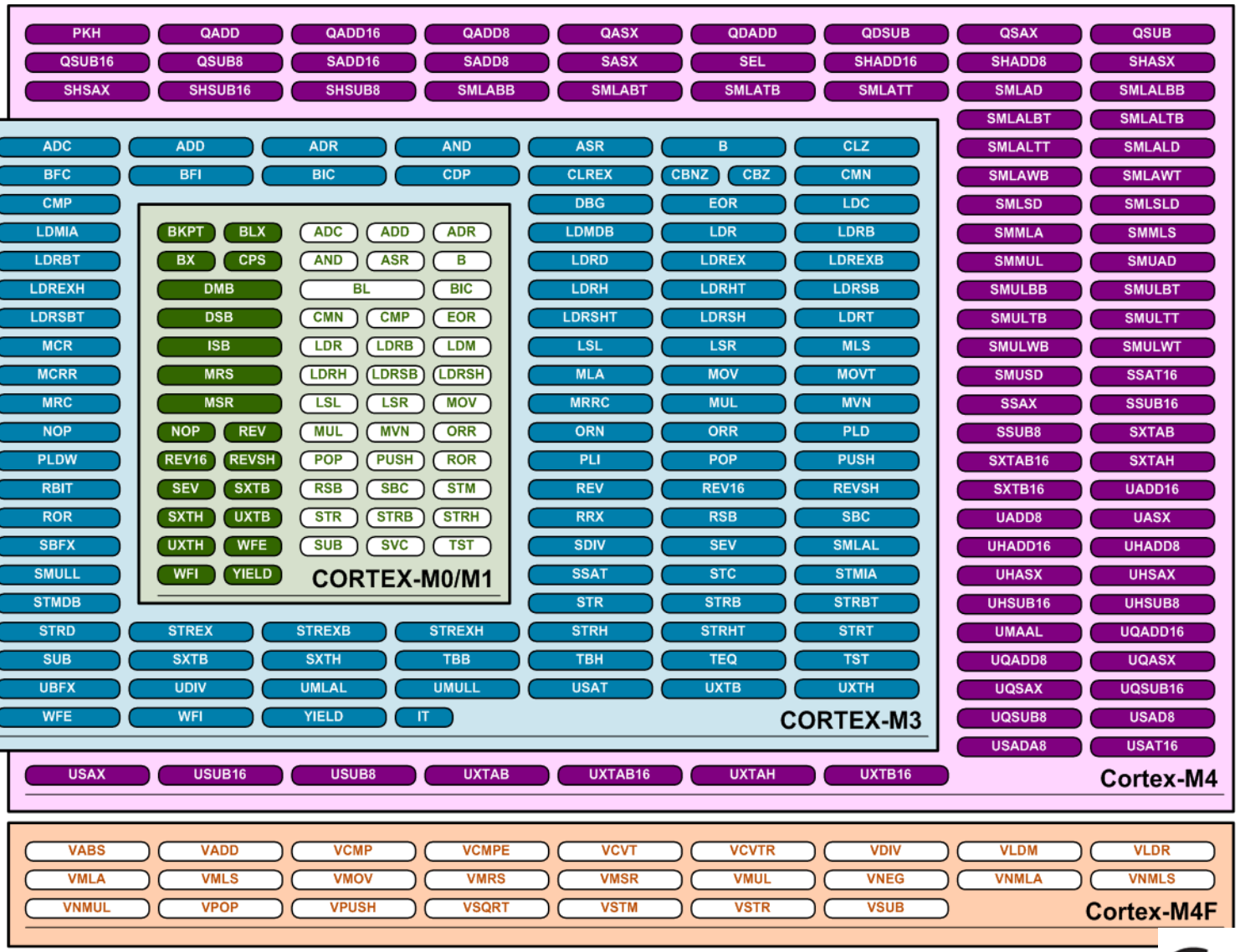
Cortex-M 处理器

- **跳出传统的8/16/32位的分类**
  - 所有应用都是无缝架构
  - 所有产品在低功耗和简易使用上都得到优化

Cortex-M0 & M0+	Cortex-M3	Cortex-M4
“8/16-bit” 应用	“16/32-bit” 应用	“32-bit/DSC” 应用

寄存器和工具兼容

Cortex-M 处理器寄存器的兼容性



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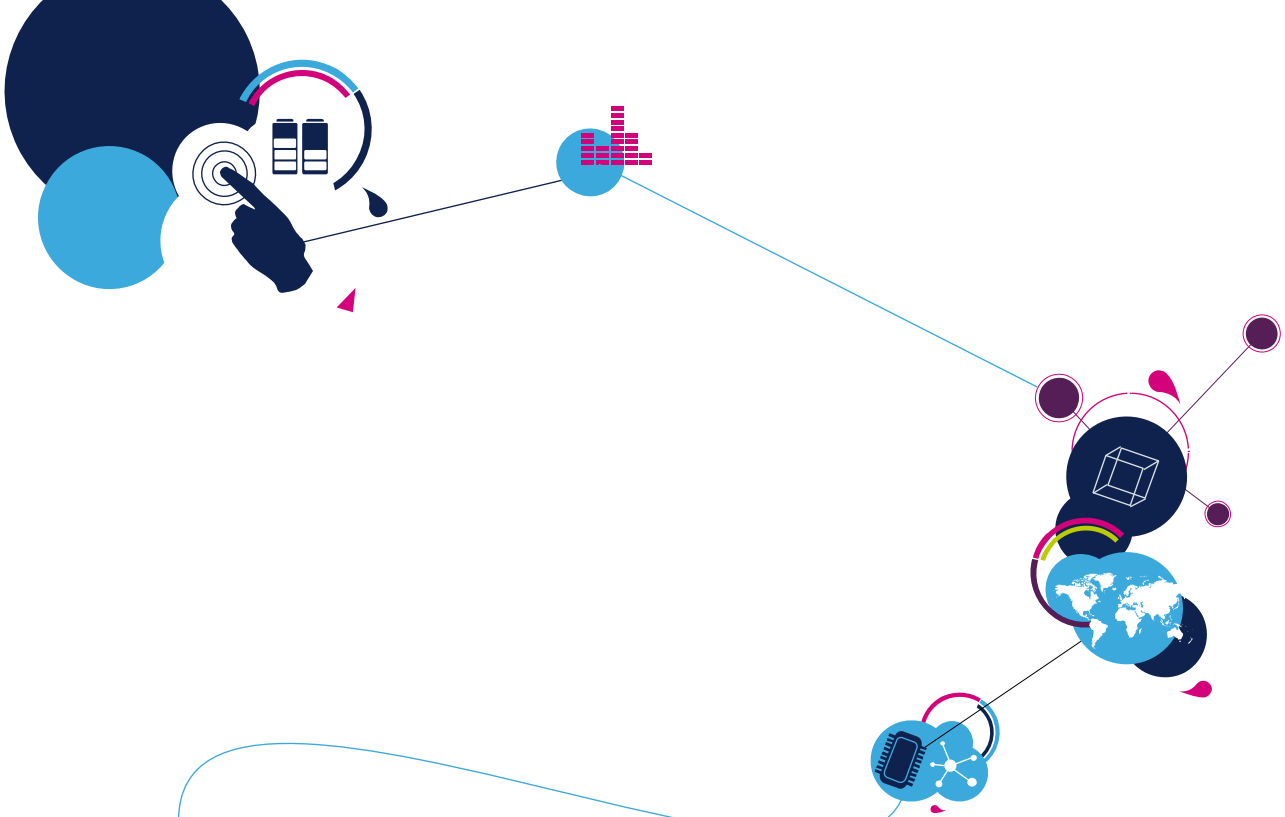
Cortex

Low-Power Leadership from ARM

Cortex-M 功能比较

	Cortex-M0+	Cortex-M3	Cortex-M4
Architecture Version	V6M	v7M	v7ME
Instruction set architecture	Thumb, Thumb-2 System Instructions	Thumb + Thumb-2	Thumb + Thumb-2, DSP, SIMD, FP
DMIPS/MHz	0.95	1.25	1.25
Bus interfaces	1+I/O port	3	3
Integrated NVIC	Yes	Yes	Yes
Number interrupts	1-32 + NMI	1-240 + NMI	1-240 + NMI
Interrupt priorities	4	8-256	8-256
Breakpoints, Watchpoints	4/2/0, 2/1/0	8/4/0, 2/1/0	8/4/0, 2/1/0
Memory Protection Unit (MPU)	Yes (Option)	Yes (Option)	Yes (Option)
Integrated trace option (ETM)	MTB (Option)	Yes (Option)	Yes (Option)
Fault Robust Interface	No	Yes (Option)	No
Single Cycle Multiply	Yes (Option)	Yes	Yes
Hardware Divide	No	Yes	Yes
WIC Support	Yes	Yes	Yes
Bit banding support	No	Yes	Yes
Single cycle DSP/SIMD	No	No	**Yes**
Floating point hardware	No	No	**Yes**
Bus protocol	AHB Lite, I/O	AHB Lite	AHB Lite
CMSIS Support	Yes	Yes	Yes

功耗



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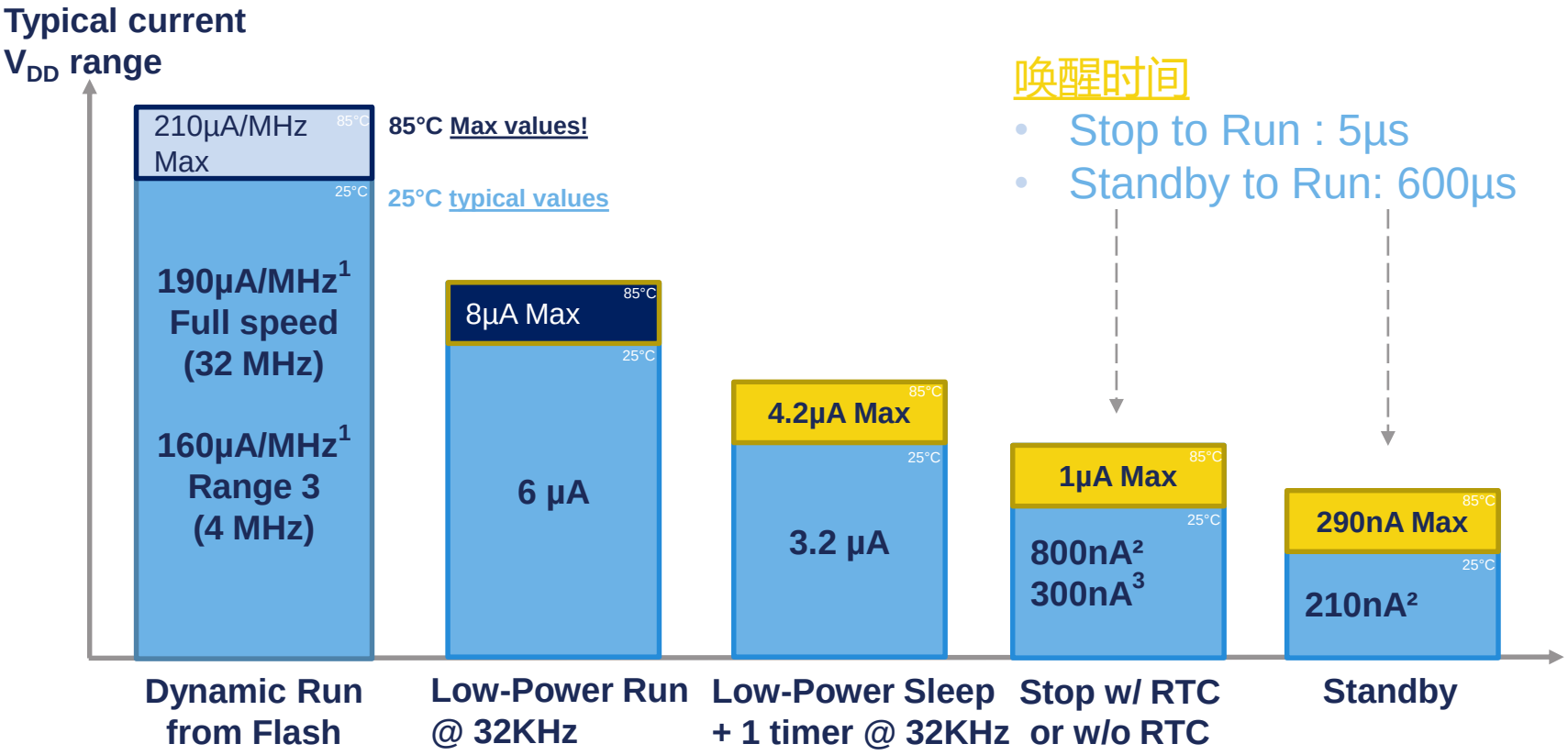
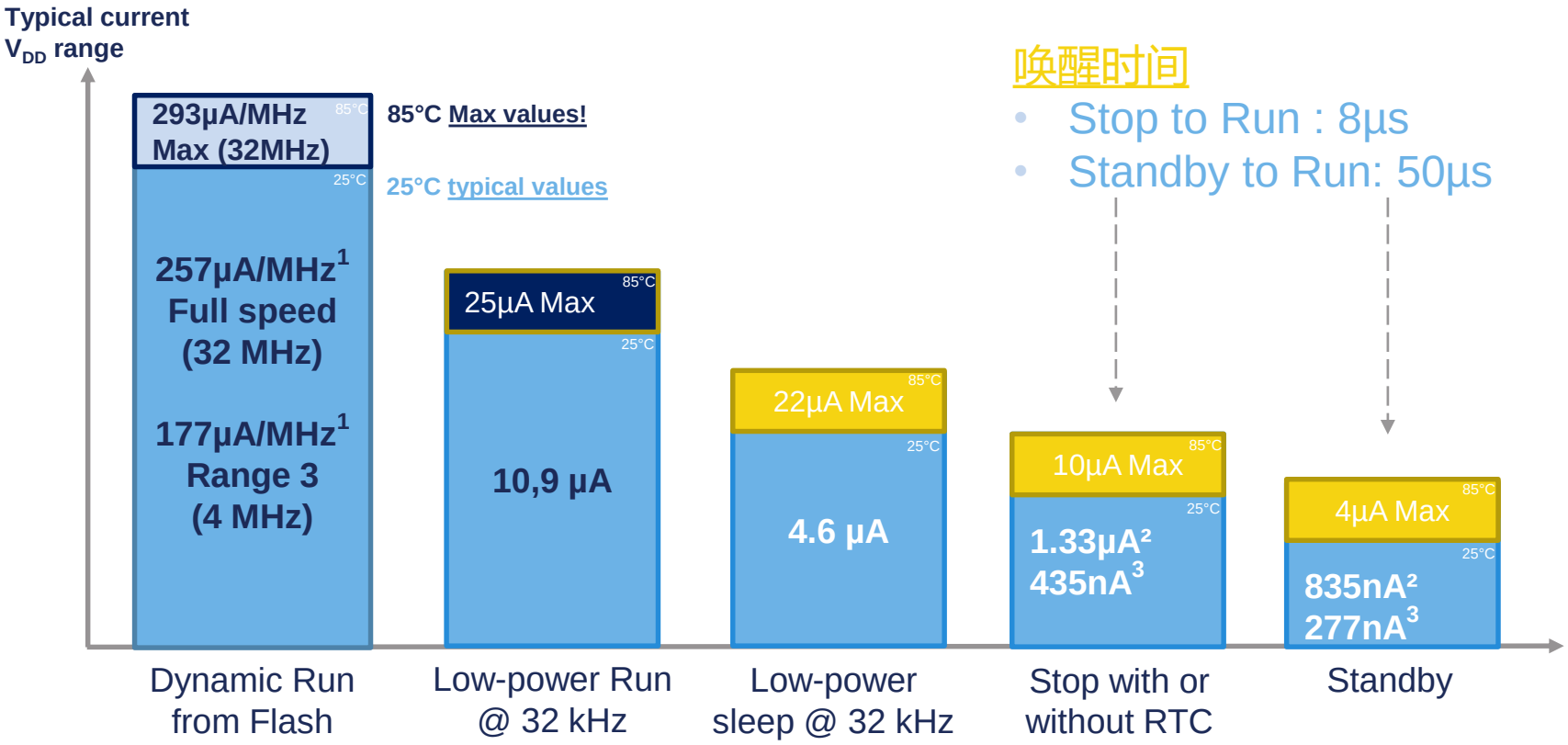
ARM

STM32L0 功耗

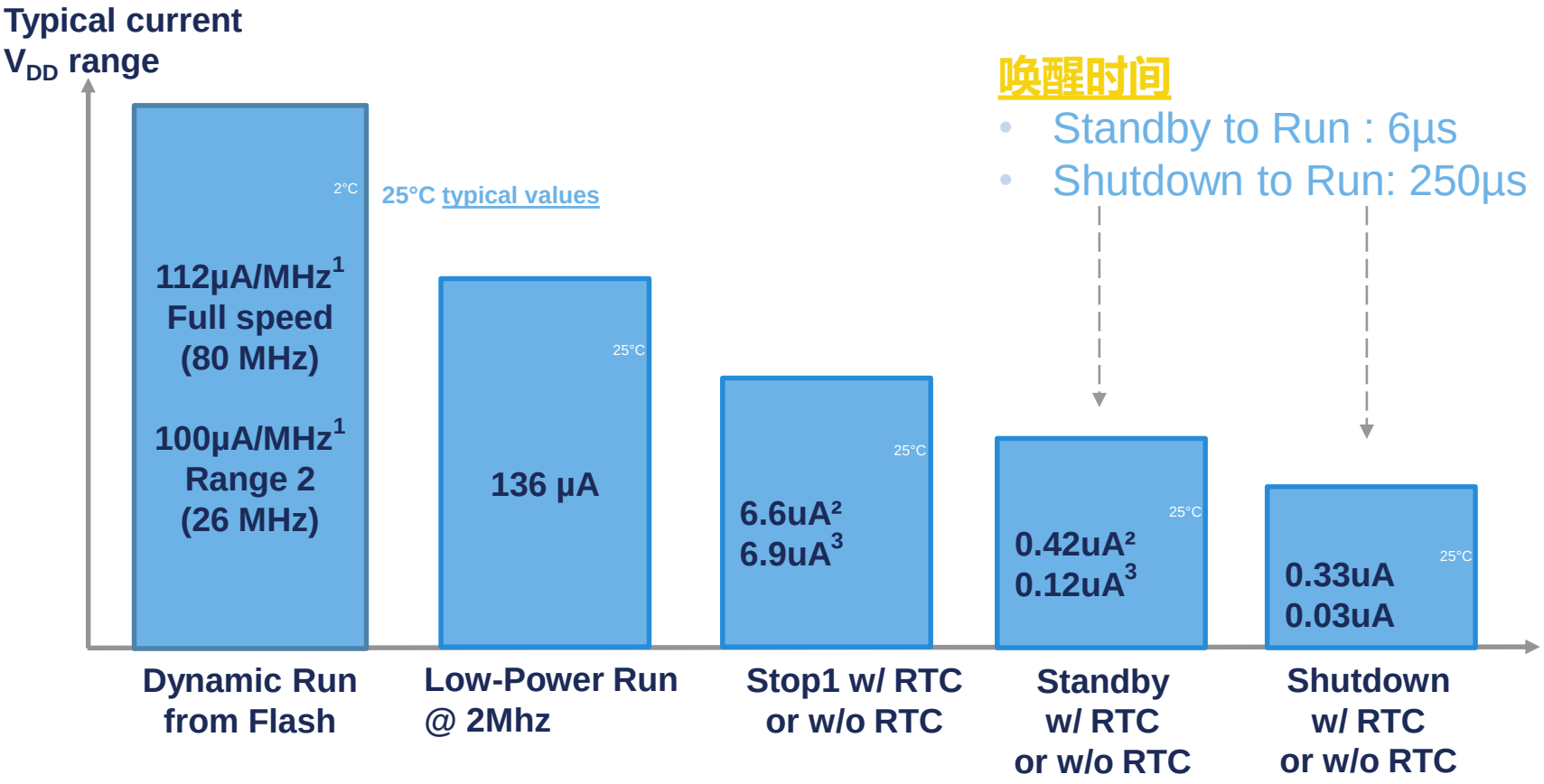

Typical current
V_{DD} range
210µA/MHz Max
85°C
25°C
85°C Max values!
25°C typical values
190µA/MHz[1] Full speed (32 MHz)
160µA/MHz[1] Range 3 (4 MHz)
8µA Max
6 µA
4.2µA Max
3.2 µA
1µA Max
800nA[2]
300nA[3]
290nA Max
210nA[2]
Dynamic Run from Flash
Low-Power Run @ 32KHz
Low-Power Sleep + 1 timer @ 32KHz
Stop w/ RTC or w/o RTC
Standby
唤醒时间
Stop to Run : 5µs
Standby to Run: 600µs

STM32L1 功耗



1. Dhrystone power consumption value executed from Flash with V_{DD} = 3V
2. Stop and Standby with RTC given with V_{DD} = 1.8V
3. Stop and Standby without RTC given with V_{DD} = 3V

STM32L4 功耗



唤醒时间

- Standby to Run : 6µs
- Shutdown to Run: 250µs

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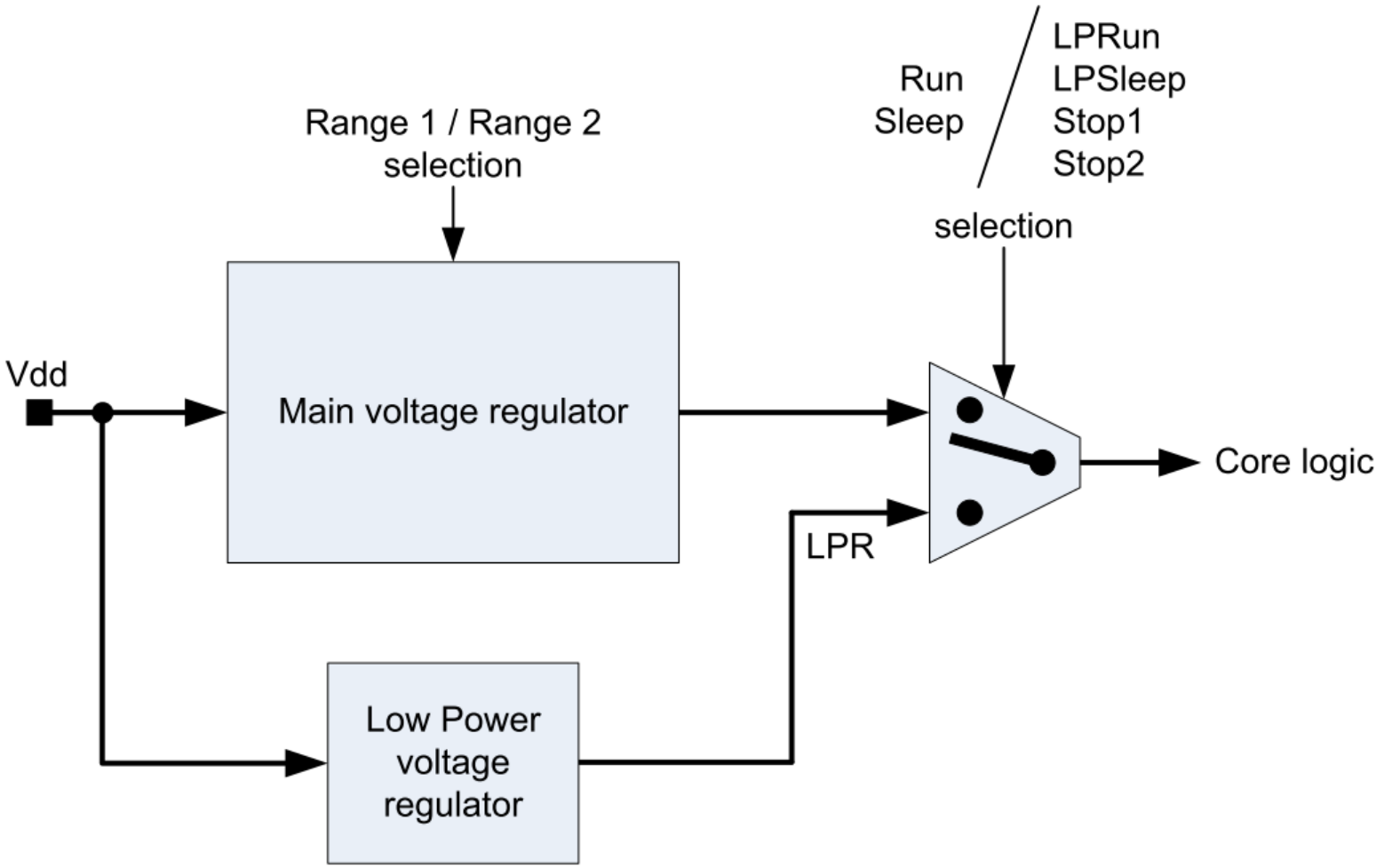
低功耗的关键

- 1:MCU的芯片大小.
  - 芯片工艺
  - 晶体管数量
  - 模拟与内部外设的使用
  - 片内RAM与FLASH的大小
- 2:MCU的供电电压
  - 当前使用的逻辑CMOS与电压成正比,所以供电电压越低,功耗越低
- 3:时钟频率
  - 时钟频率越低,功耗越低
- 4:工作模式
  - 功耗依赖于不同的工作模式,因为不同的工作模式下,CPU、时钟、外设等的工作情况不一样

电源部分

- 主电源电压转换器
- 低功耗电压转换器



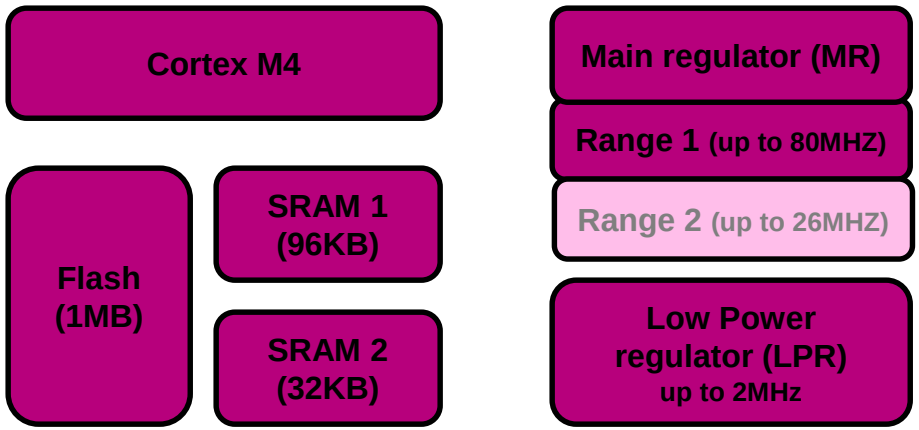
MCU的工作模式

- 以STM32L4为例子
  - Low-power run and Low-power sleep modes
  - STOP mode
  - STANDBY mode
  - SHUTDOWN mode

STM32L4 功耗模式

Run 模式

Run 模式Range 1
Ex: 从内部Flash执行



Range 1
127uA/MHz at 80 MHz
(10.2mA)

Range 2
111uA/MHz at 26 MHz
(2.9 mA)

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

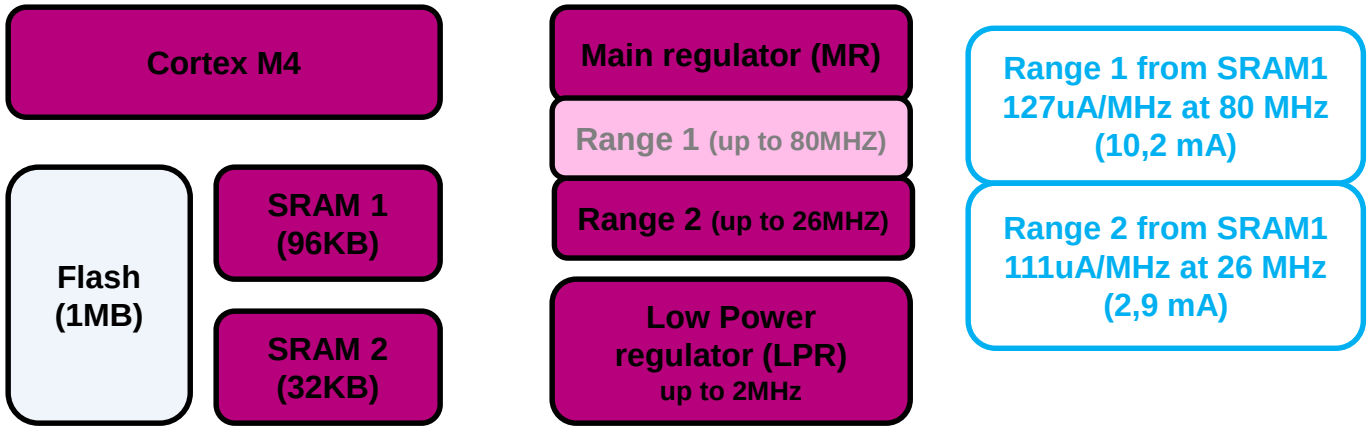
Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 功耗模式
Run 模式

Run 模式Range 2
Ex: 从内部SRAM执行



Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Run 和Low-power run 模式

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory
  - Device software configuration
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash or SRAM
    - When execution from Flash: ART accelerator configuration (Cache, Prefetch)
    - When execution from SRAM: SRAM1 or SRAM2

Run and Low-power run modes

- When executing from Flash, the best configuration is:
  - I-CACHE ON, D-CACHE ON, PREFETCH **OFF**

		ART ON (Cache ON, Prefetch Off)	ART OFF
Range 1@80MHz (4 WS)	Consumption(mA/MHz)	0,136	0.117
	Performance (Coremark/MHz)	3.32	1,55
	Energy Efficiency (Coremark/mA)	**24.4**	13.2
Range 2@26MHz (3 WS)	Consumption(mA/MHz)	0,118	0,111
	Performance (Coremark/MHz)	3.35	1,85
	Energy Efficiency (Coremark/mA)	**28,4**	16,6

Run and Low-power run modes

- When executing from SRAM, the best configuration is:
  - Execution from SRAM2

		Code & Data in SRAM1	Code in SRAM2, Data in SRAM1
Range 1@80MHz	Consumption(mA/MHz)	0,130	0.137
	Performance (Coremark/MHz)	2,37	3,42
	Energy Efficiency (Coremark/mA)	18,2	**25,0**

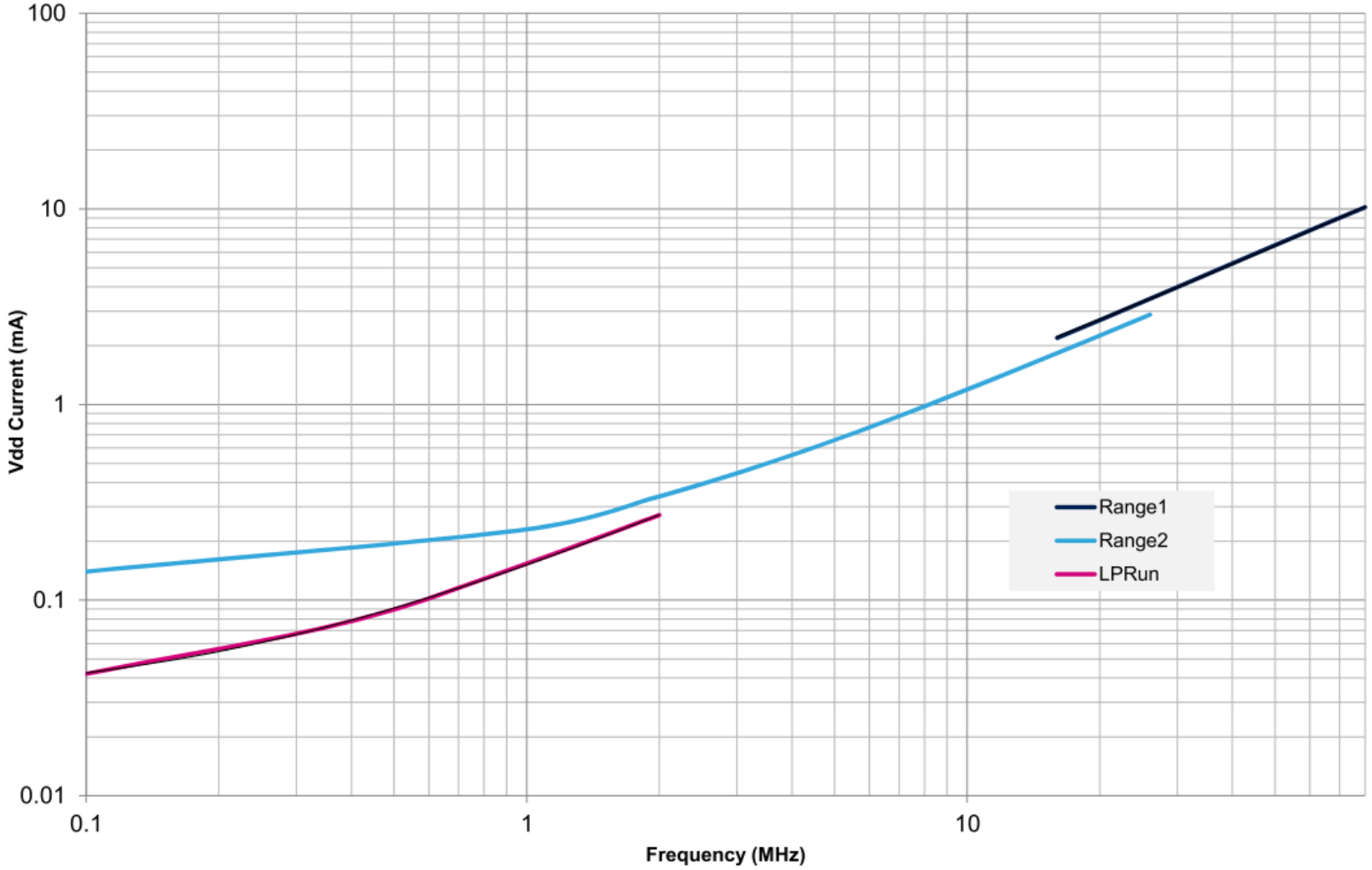
Low-power run mode

- Max system frequency is **2MHz**
- **Execution from Flash or Ram**
- **Peripheral clock can be HSI**

	100 kHz	2 MHz
Execution from Flash	42 µA	272 µA
Execution from SRAM1	26 µA	242 µA

Low-power run	Description
Mode entry	Decrease the system clock frequency below 2 MHz Force the regulator in low-power mode : set **LPR** in PWR_CR1
Mode exit	LPR = 0 Wait until REGLPF = 0 in PWR_SR2 Increase the system clock frequency
Wakeup latency	Regulator wakeup time from low-power mode

电流VS系统时钟



各组合下的运算能力

Table 2. STM32L476 performance for different Run modes

Run mode	Configuration	mA/MHz	CoreMark® per MHz	CoreMark® per mA
Range 1 (80 MHz)	FLASH ART Off	0.117	1.55	13.2
	FLASH ART On	0.136	3.32	24.4
Range 2 (26 MHz)	FLASH ART Off	0.111	1.85	16.6
	FLASH ART On	0.118	3.35	28.4

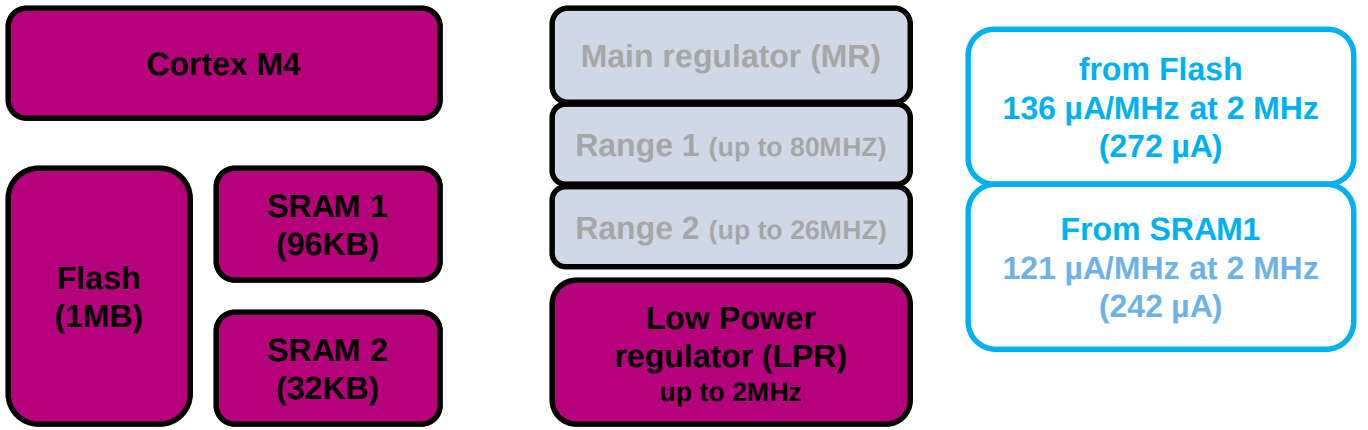
STM32L4 Power Mode

Low-power run mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Low-power run mode
Ex: execution from Flash



Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Sleep and Low-power sleep modes

- **Sleep and Low-power sleep mode**: Core stopped, peripherals kept running
  - Entered from by executing special instructions
    - **WFI** (Wait For Interrupt)
      - Exit: any peripheral interrupt acknowledged by the Nested Vectored Interrupt Controller (NVIC)
    - **WFE** (Wait For Event)
      - An *event* can be an interrupt enabled in the peripheral control register but NOT in the NVIC or an EXTI line configured in event mode
      - Exit: as soon as the event occurs ➔ No time wasted in interrupt entry/exit
  - Two mechanisms to enter this mode
    - **Sleep Now**: MCU enters SLEEP mode as soon as WFI/WFE instruction are executed
    - **Sleep on Exit**: MCU enters SLEEP mode as soon as it exits the lowest priority ISR
      - The stack is not popped before entering the sleep, it will not be pushed when the next interrupt occurs, saving running time
    - **Controlled by CortexM4 reg System Control Register[SLEEPONEXIT]**

Sleep and Low-power sleep modes

- Entered by executing WFI or WFE either when
  - Main regulator is ON => Sleep mode
  - Main regulator is OFF => Low-power sleep mode

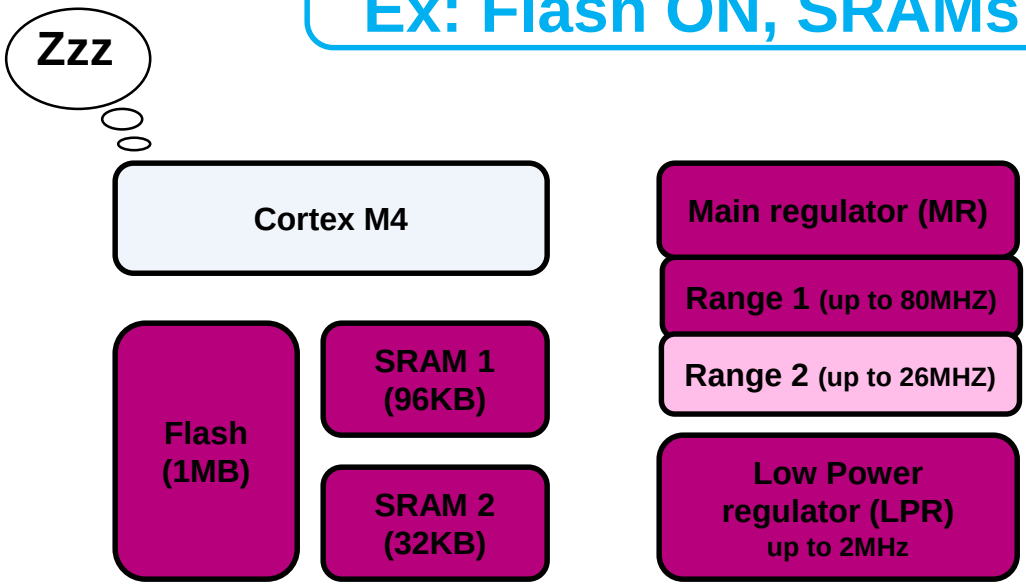
- Each peripheral clock can be configured to be ON or OFF in Sleep or Low-power sleep modes thanks to RCC_AHB1SMENR, RCC_AHB2SMENR, RCC_AHB3SMENR, RCC_APB1SMENR1, RCC_APB1SMENR2, RCC_APB2SMENR
  - For the peripherals with independent clock : the bit controls both AHB/APB and kernel clock
  - This bit controls also the kernel clock in Stop mode

- **By default, FLASH, SRAM1 and SRAM2 clocks are ON in Sleep or Low-power sleep modes**
  - They can be disabled during Sleep/Low-power sleep by clearing **FLASHSMEN**, **SRAM1SMEN**, **SRAM2SMEN**
  - Flash can be put in power-down during Sleep/Low-power sleep by setting **SLEEP_PD** in FLASH_ACR

STM32L4 Power Mode

Sleep mode

Sleep Mode Range 1
Ex: Flash ON, SRAMs ON (default)



Range 1
37 µA/MHz at 80 MHz
(2,96 mA)

Range 2
35 µA/MHz at 26 MHz
(0,92 mA)

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
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- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available Clock

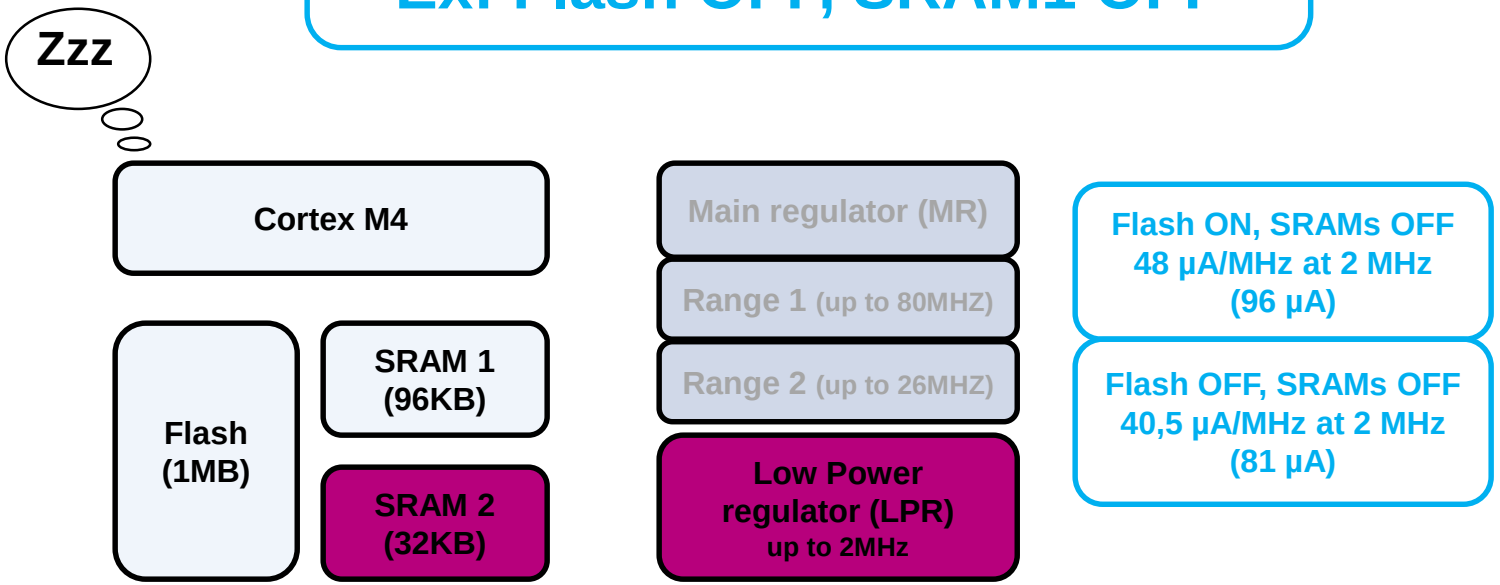
- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Low-power sleep mode

Low-power sleep mode
Ex: Flash OFF, SRAM1 OFF



Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
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- RNG
- AES
- CRC

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Batch Acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power.

1. Only the needed communication peripheral + 1 DMA + 1 SRAM (SRAM1 or SRAM2) are configured with clock enable in Sleep mode

2. Flash is put in power-down mode and Flash clock is gated off during Sleep

3. Enter either Sleep or Low-power sleep mode
   - Note that I2C clock can be at 16 MHz even in low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI.

Low-power modes

- Next low-power modes are selected with **LPMS** in PWR_CR1
  - LPMS = 000 : Stop 1 mode selection with regulator in main mode
  - LPMS = 001 : Stop 1 mode selection with regulator in low-power mode
  - LPMS = 010 : Stop 2 mode selection
  - LPMS = 011 : Standby mode selection
  - LPMS = 1xx : Shutdown mode selection
- Before entering Stop 2 mode :
  - All the peripherals which cannot be enabled in Stop 2 mode must be either disabled by clearing the Enable bit in the peripheral itself, or put under reset state through control bit in the RCC

STM32L4 Power Mode

Stop 1 Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os kept, and configurable

Stop 1 w/ RTC on LSE quartz → **7,9 µA @3.0V**
7.6 µA @1.8V

Zzz

Cortex M4

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Main regulator (MR)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

6us wake-up from Flash
4us wake-up from RAM

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Stop 1 Mode

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Stop 1 w/o RTC ⇨ **7,5 µA @ 3.0V**
7.3 µA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

6us wake-up from Flash
4us wake-up from RAM

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Stop 2 Mode

Stop 2 w/ RTC on LSE quartz ⇨ **1.66 µA @3.0V 1.43 µA @1.8V**

Zzz

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Cortex M4

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Main regulator (MR)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

7us wake-up from Flash
5us wake-up from RAM

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Stop 2 Mode

Stop 2 w/o RTC ⇨ **1.25 µA @3.0V**
1.19 µA @1.8V

Zzz

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
- Backup Register (32x32-bits)
- RTC

7us wake-up from Flash
5us wake-up from RAM

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Stop 1 & Stop 2 modes

	STOP1 mode		STOP2 mode	
Consumption (datasheet)	25°C	85°C	25°C	85°C
	7.46 µA w/o RTC 7.93 µA w/ RTC	105 µA w/o RTC 107 µA w/ RTC	1.25 µA w/o RTC 1.66 µA w/ RTC	16.4 µA w/o RTC 17.2 µA w RTC
Wakeup time	6µs in Flash 4µs in RAM		7 µs in Flash 5 µs in RAM	
Wakeup clock	MSI configurable **up to 48MHz** Or HSI at 16MHz, selected with **STOPWUCK** in RCC_CFGR			
Peripherals	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG			
	USB (suspend, ADP) 2 LP TIMERs 1 LP UART 3 I2C 5 UARTx SWPMI(resume from suspend)		1 LP TIMER (**LPTIM1**) 1 LP UART 1 I2C (**I2C3**)	

STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby w/ SRAM2 w/o RTC

405 nA @ 3.0V
363 nA @1.8V

Zzz

Cortex M4

Main regulator (MR)

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- BOR
- RTC + Tamper
- IWDG
- 5 WKUP pins

14 us wake-up

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby w/ RTC on LSE quartz → **674 nA @ 3.0V**
433 nA@ 1.8V

Zzz

- Cortex M4
- Main regulator (MR)
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Low Power regulator (LPR)
- Backup domain
- Backup Register (32x32-bits)
- RTC

Wake-up event

- NRST
- BOR
- RTC + Tamper
- IWDG
- 5 WKUP pins

14 us wake-up

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby ⇨ **169 nA @ 3.0V**
128 nA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Main regulator (MR)
- Low Power regulator (LPR)
- **Backup domain**
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- **NRST**
- **BOR**
- **RTC + Tamper**
- **IWDG**
- **5 WKUP pins**

14 us wake-up

Available Clock

- HSI
- HSE
- **LSI**
- **LSE**
- MSI

Active cell | **Frozen cell** | Cell in power-down | **Available Periph and clock**

Standby mode

- Ultra Low Power **BOR** always ON (V_{BOR0})
  - Higher thresholds brings additional consumption
- Configurable **pull-up or pull-down on all I/Os**
  - PWR_PUCRx registers (x = A,B,…H)
  - PWR_PDCRx registers (x = A,B,…H)
  - Configuration applied when **APC** is set in PWR_CR3 register.
- Possibility to **backup 32kbytes SRAM2**
  - Set **RRS** bit in PWR_CR3 register
- 128 bytes backup registers
- The polarity of each of the **5** wakeup pins is configurable
- Wakeup clock is **MSI configurable from 1 to 8MHz**.

Shutdown mode : 新功能!

- 类似于standby mode 但是 **没有电源监控** : no BOR/PVD, no switch to VBAT, no LSI , no IWDG
- 128 字节 备份寄存器
- 唤醒源: **5** wakeup pins, RTC
- **功耗 30nA w/o RTC**, 0.8 µA w/ RTC
- **唤醒时间 500µs** . 唤醒时钟MSI 可以配置 1 到 8MHz.

STM32L4 Power Mode
Shutdown Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

Shutdown w/ RTC on LSE quartz → **476 nA @ 3.0V**
265 nA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- NRST
- RTC + Tamper
- 5 WKUP pins

250 us wake-up

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

STM32L4 Power Mode

Shutdown Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

Shutdown ⇨ **77 nA @ 3.0V**
43 nA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- NRST
- RTC + Tamper
- 5 WKUP pins

256 us wake-up

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell	Frozen cell	Cell in power-down	Available Periph and clock

Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals In Bold : wakeup source	Consumption @ 1.8V	Wakeup time
Run	R1	Yes	ON(1)	ON	Any	All	127 µA/MHz	N/A
	R2					All except OTG, SDMMC, RNG	111 µA/MHz	
LPRun	LPR	Yes	ON(1)	ON	Any *except PLL*	All except OTG, SDMMC, RNG	136 µA/MHz	TBD
Sleep	R1	No	ON(1)	ON(2)	Any	All **Any IT or event**	37 µA/MHz	6 cycles
	R2						35 µA/MHz	
LPSleep	LPR	No	ON(1)	ON(2)	Any *except PLL*	All except OTG, SDMMC, RNG **Any IT or event**	40 µA/MHz	6 cycles
Stop 1	LPR	No	OFF	ON	LSE/LSI	**Reset pin, all I/Os** **BOR,PVD,PVM,RTC,LCD,IWDG,** **COMPx**,DACx,OPAMPx,**USARTx,** **LPUART,I2Cx,LPTIMx,OTG_FS,** **SWPMI**	7.3µA w/o RTC 7.6 µA w/RTC	4 µA RAM 6 µA Flash
Stop 2	LPR	No	OFF	ON	LSE/LSI	**Reset pin, all I/Os** **BOR,PVD,PVM,RTC,LCD,IWDG,** **COMPx,LPUART,I2C3,LPTIM1**	1.2 µA w/o RTC 1.4 µA w/RTC	5 µA RAM 7 µA Flash
Standby	LPR	DOWN	OFF	SRAM2 ON	LSE/LSI	**Reset pin, 5 WKUPx pins** **BOR, RTC, IWDG**	+ 235 nA	14 µs
	OFF			DOWN			128 nA w/o RTC 433 nA w/RTC	
Shutdown	OFF	DOWN	OFF	DOWN	LSE	**Reset pin, 5 WKUPx pins** **RTC**	43 nA w/o RTC 265 nA w/RTC	256 µs

1. Can be put in power-down and clock can be gated off
2. SRAM1 and SRAM2 can be gated off independently

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市场应用

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ARM

目标市场

ULP at the heart of all energy concern

- Wellness / Fitness / Lifestyle
  - Activity trackers, GPS, Smart watch, glasses

- Home automation
  - Thermostat, alarm detector, in-home display

- Metering
  - Gas, water, Electricity

- Industrial
  - Sensors, 4-20 mA loop
- Medical
  - Insulin pump, Glucosemeter

- Safety
  - Mobile POS

STM32L4 whatever the application

Smart peripherals
Metering

Digital **F**ilter for **S**igma **D**elta **M**odulators
8 x parallel inputs
with up to 24-bit data
output resolution

LCD Display

88×40 or 4×44
with step-up converter

VBAT with RTC
for battery backup
240 nA in VBAT mode
for RTC and
32x 32-bit backup registers

STM32L4

Electricity/Gas /Water Smart Meter

Anti Tamper pin
3 x tamper pins
for battery domain

TRNG & AES
for Security
128-/256-bit AES
key encryption hardware
accelerator

SPI / UART/ SDIO for Wireless
3x SPIs (4x SPIs with the Quad SPI)
6x USARTs (ISO 7816, LIN, IrDA, modem)
1 x SDIO

FSMC
External memory interface
for static memories supporting SRAM,
PSRAM, NOR and NAND

I/Os Up to 114 fast I/Os for buttons & relays

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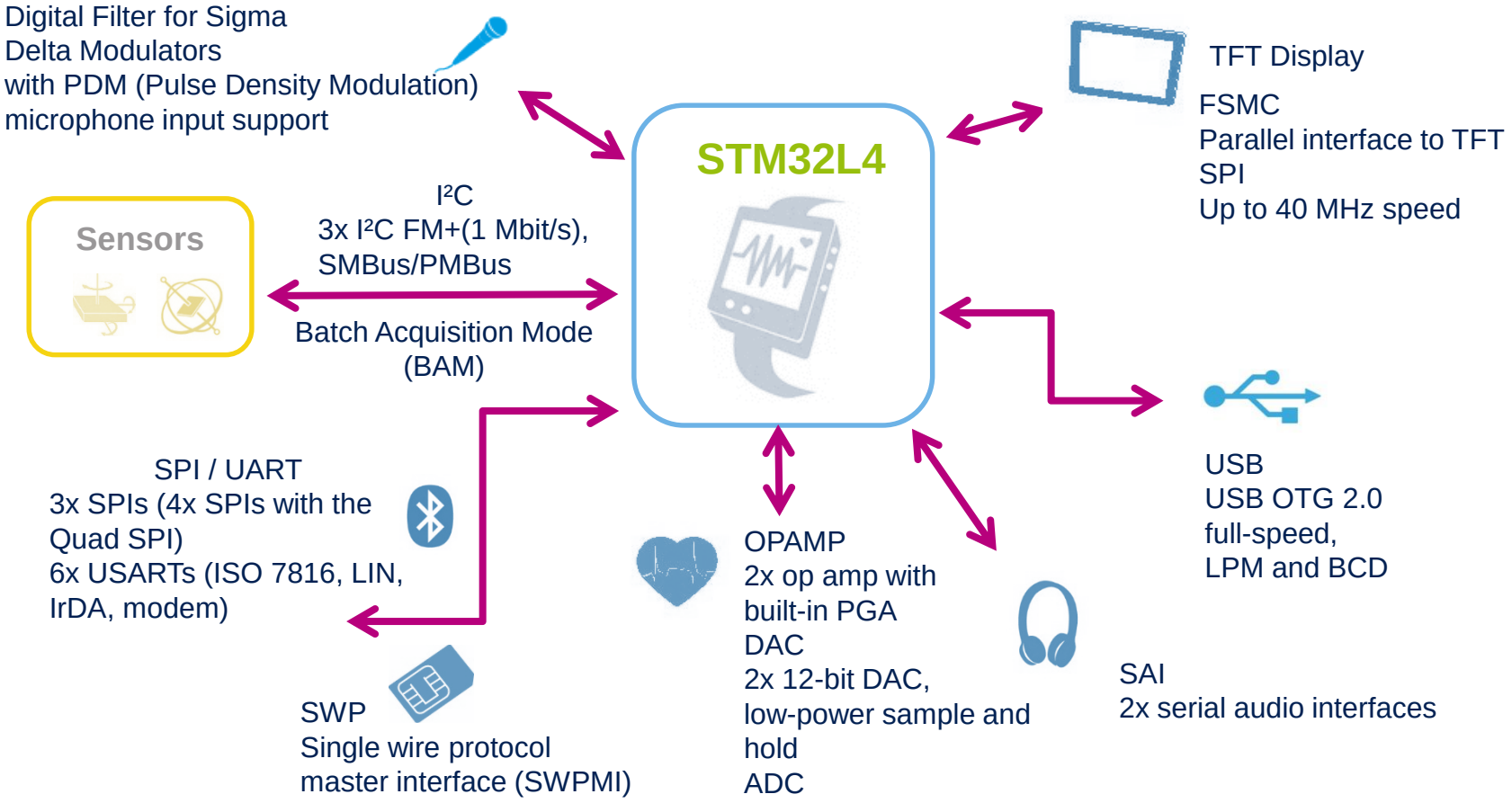
Smart peripherals
Fitness tracker - Wristband



Smart Peripherals
Industrial Sensors

Motor Control :
2x 16-bit advanced
motor-control timers
3x 12-bit ADCs: 5 MSPS,
with up to 16-bit with hardware
oversampling, 200 µA/MSPS

LCD Display

8×40 or 4×44
with step-up converter

CAN Bus
(2.0B Active)

STM32L4

High temperature
from -40°C
up to + 125°C

TRNG & AES
for Security
128/256-bit AES
key encryption hardware accelerator

SPI / UART
3x SPIs (4x SPIs with the
Quad SPI)
6x USARTs (ISO 7816, LIN,
IrDA, modem)

FSMC
External memory interface
for static memories supporting
SRAM, PSRAM, NOR and NAND

Accurate RC Oscillator
+/-1% over temperature

I²C
3x I²C FM+(1 Mbit/s), SMBus/PMBus

Digital Smart Peripherals

- Peripherals running in Stop mode
  - Low-power UART can wake up the system if a programmed byte or start bit is detected (with no loss of the first bit)
  - I²C can wake up system when address is detected
  - Low-power timer can count time or events or generate signals
- Quad SPI for data and execution in place
- Digital Filter for Sigma Delta Modulator
  - For connection to external sigma delta modulator (e.g.: STPMS2)
  - Up to 4 filters, 8 multiplexed channels
  - Also supports digital microphone MEMs (PDM to PCM conversion and filtering performed by HW)
- Peripheral clock independent from main system clock
- Single Wire Protocol interface for smartcards

Analog Smart Peripherals

- 3 x 12/16-bit ADCs (up to 5 Msps)
  - adaptive power consumption (200µA/ Msps)
  - HW oversampling
  - Single and differential inputs
- 2x Op amps with built-in PGA
- 2 x 12-bit DACs (1 Msps)
  - Low-power Sample and Hold modes available in Stop mode
- 2x Comparators
  - Low-power modes, works in Stop mode
- Internal voltage reference
  - Programmable 2.048 or 2.5 V
  - Can be used for external components

生态环境

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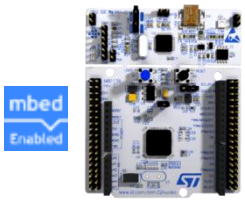
ARM

STM32L4 ecosystem

HARDWARE TOOLS

STM32 Nucleo



Flexible prototyping

Discovery kit

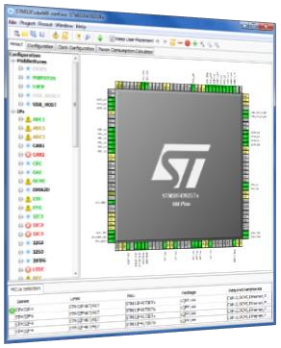
Key feature prototyping

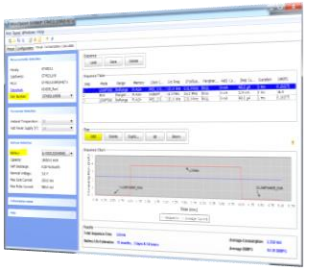
Evaluation board

Full feature evaluation

SOFTWARE TOOLS

STM32CubeMX featuring code generation and power consumption calculation





BAM + 典型应用

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Batch Acquisition mode (BAM)

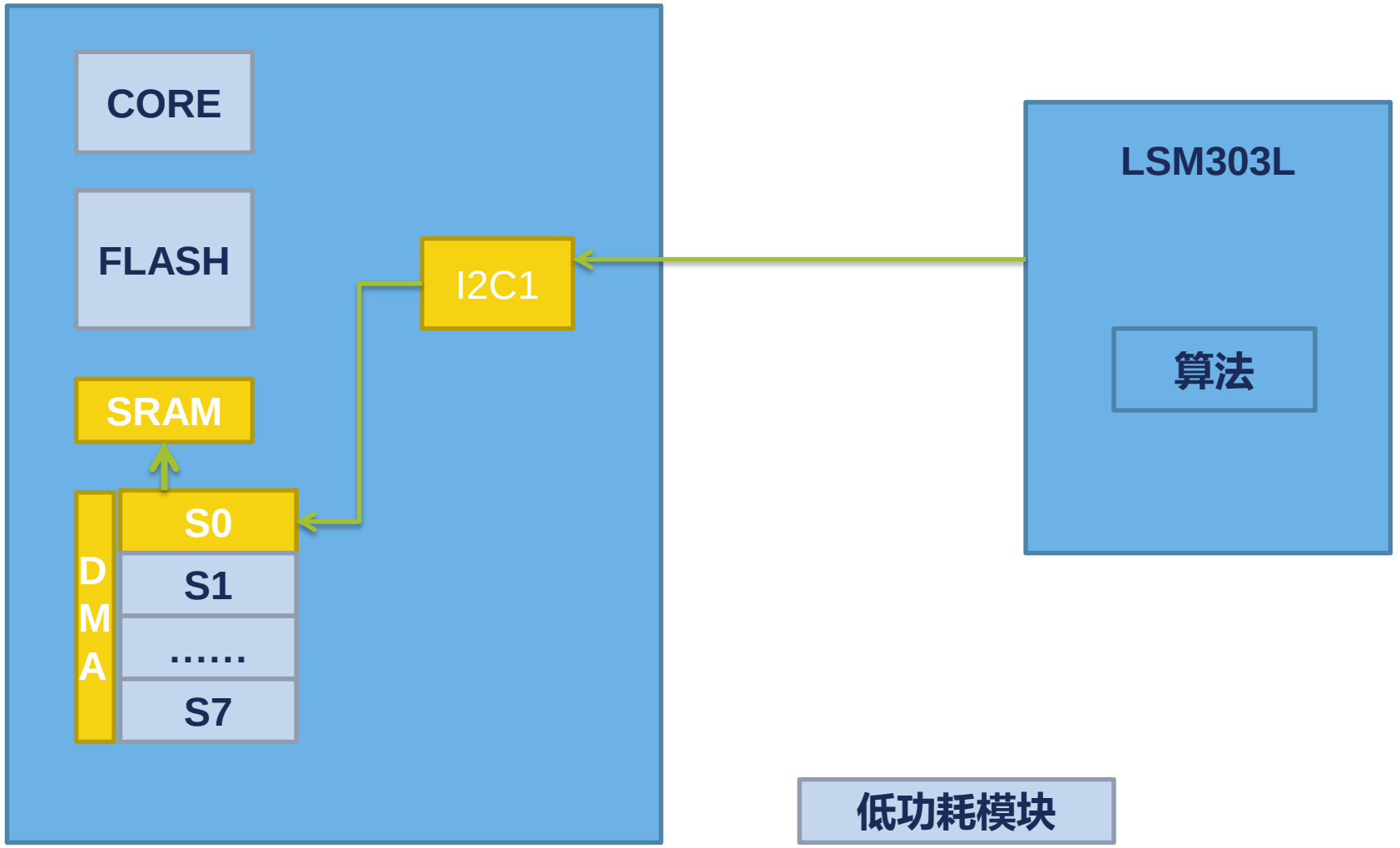
最佳化模式:在低功耗模式下,通过外设进行数据通信.

1. 只选择所需的外设 + 1 DMA + 1 SRAM (SRAM1 or SRAM2) 在Sleep mode下配置时钟使能

2. Flash 设置为power-down 模式和FLASH时钟在睡眠状态下关闭

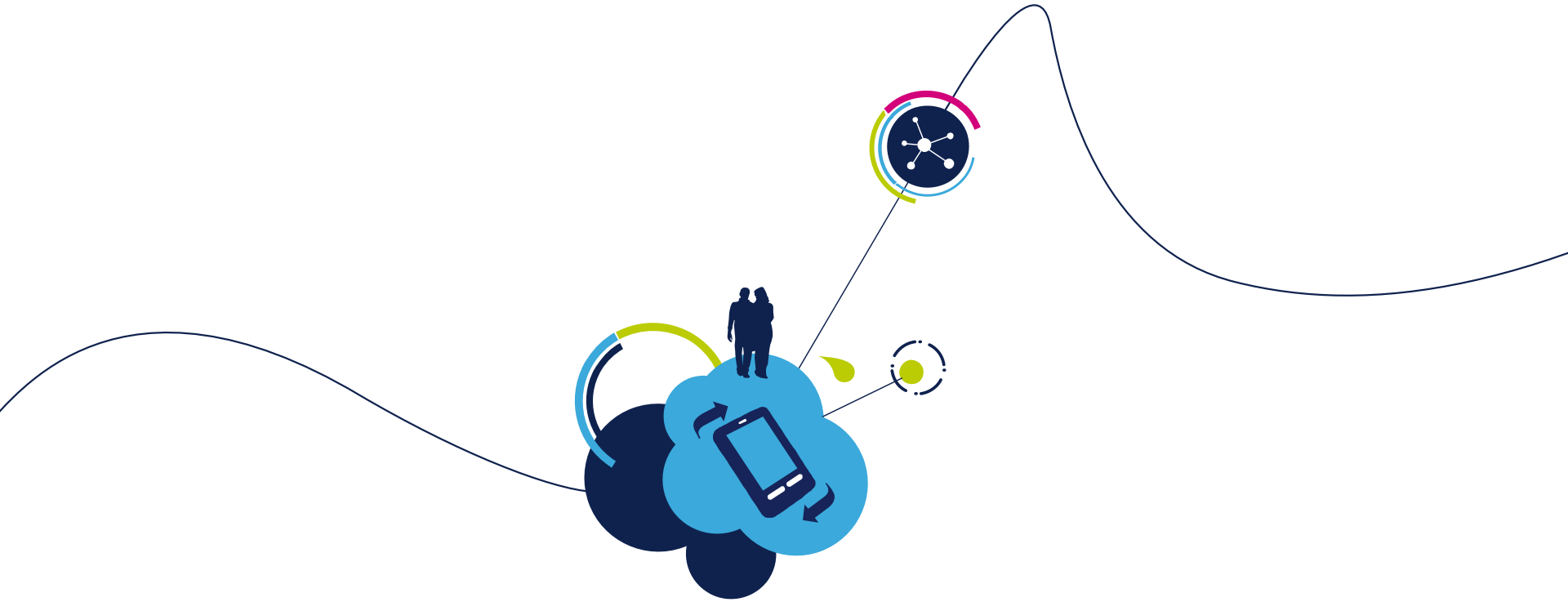
3. 进入睡眠模式或者低功耗睡眠模式
   - 注意I2C时钟可以设置16Mhz,甚至在低功耗睡眠模式下,允许1Mhz 的加强快速模式. U(S)ART/LPUART 时钟可以是HSI.

BAM典型应用



Low Power总结

- 选用低电压
- 选用适当的频率
- 正确的打开指令预取
- 在低功耗下，根据应用，适当的关闭FLASH
- 根据具体应用，平衡BAM与STOP mode之间的取舍
- 在lowpower下，将没用的GPIO设置成AN mode
- 根据主频的速率，可以调整内核电压。



谢谢

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备用

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
RCC	部分兼容	部分兼容
DMA	全兼容	
Interrupt	兼容	
GPIO	全兼容	

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	不兼容	N/A
C		兼
DI		全兼
Interrupt	兼容	
GPIO	全兼容	

读操作:word,half-word或byte
写操作:word 或 half
ECC:每个word有6bit ecc.可以纠正一个byte的错误
EEPROM:2KB 带 ECC
读写保护
低功耗功能

读操作:word 或dual word
写操作:word 或 half
ECC:每个word有6bit ecc.可以纠正一个byte的错误
EEPROM:2KB~ 16KB带 ECC
读写保护
低功耗功能

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全	N/A
CRC		
PWR		
RCC		
DMA		
Interrupt	兼容	
GPIO	全兼容	

读写操作:72bit
读写保护:四个写保护,两个读保护
预存取
ECC:两个word有8bits ecc,可以纠正一个byte的错误
低功耗

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC		兼容
PWR		
RCC		
DMA		
Interru		
GPIO		全兼容

可以对RAM和FLASH进行指定区域进行操作权限访问.

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
RCC	部分兼容	
DMA		
Interrupt		
GPIO	全兼容	

多项式:固定0x4C11DB7
单寄存器输入输出32bit数据
计算时间:4个AHB时钟周期

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	容	部分兼容
R		
D		
Interr		
GPIO	全兼容	

多项式:可编程
数据长度:8-,16-,32bit长度
CRC初始值:可编程
单寄存器输入输出32bit数据
计算时间:4个AHB时钟周期

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
RCC	部分兼容	
DMA		
Interrupt		
GPIO		全兼容

模式:run,sleep,stop和standby模式

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
	部分兼容	部分兼容
		兼容
		容
		兼容

模式:run,sleep,stop,standby和 shutdown 模式

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
RCC	部分兼容	部分兼容
DMA		
Interrup		
GPIO		

RCC:NRST,WWDG,IWDG,SW reset,LP reset,option byte loader reset,exit from standby mode,**firewall protection**

RCC:NRST,WWDG,IWDG,SW reset,LP reset,option byte loader reset,exit from standby mode

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼	
CRC	全兼	
PWR	部分	
RCC	部分	
DMA	全兼容	
Interrupt	兼容	
GPIO	全兼容	

每个通道都支持软件触发
每个通道支持四个优先级
支持byte,half word和word四个发送尺寸
支持循环缓存管理
支持内存到内存,外设到内存,内存到外设和外设到外设.

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容
PWR	部分	
RCC	部分	
DMA		
Interrupt	兼容	
GPIO	全兼容	

可屏蔽的中断通道
可编程的优先等级
低延迟异常和中断处理
电源管理控制

全系列功能的兼容性

STM32L4 外设	From STM32L0	From STM32L1
Cortex M4 with FPU	Cortex M0+ (no FPU/DSP)	Cortex M3 (no FPU/DSP)
Flash	不兼容(eeprom)	不兼容(eeprom)
Firewall	全兼容	N/A
CRC	全兼容	兼容 有新功能
PWR	部分兼容	部分兼容
RCC	部分兼容	部分兼容
DMA	全兼容	
Interrupt	兼容	
GPIO	**全兼容**	

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分兼容 New features
LPUART	全兼容	N/A
CAN	N/A	N/A
SAI	N/A	N/A
SDIO	N/A	全兼容 + Bug fixes
USB OTG FS	不兼容 (no OTG on L0)	不兼容 (no OTG on L1)
SWPMI	N/A	N/A

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	兼容 features	部分 New
US		
LP		
C		
S		
SI		
USB OTG FS	不兼容 (no OTG on L0)	不兼容 (no OTG on L1)
SWPMI	N/A	N/A

NEW:
加强快速模式:1Mhz
独立时钟
唤醒MCU于stop mode下

标准速度:100kHz
快速:400kHz
模拟噪音滤波器
两个从设备地址
SMBus 2.0
两个中断向量
1个byte的DMA缓存

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分
LPUART	全兼容	
CAN	N/A	
SAI	N/A	
SDIO	N/A	
USB OTG FS	不兼容 (no OTG on L0)	不兼容 (no OTG on L1)
SWPMI	N/A	N/A

三线的全双工同步通信
8bit或16bit的传输帧格式选择
主从模式切换
主从模式下的快速通信
MSB和LSB格式选择

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分兼容 New features
		A
		A
		A
		兼容 Bug fixes
OTG FS	(no OTG on L0)	不兼容 (no OTG on L1)
SWPMI	N/A	N/A

NEW:
32bit的发送接收FIFO缓存
数据打包
NSSP模式

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分兼容 New features
LPUART	全兼容	N/A
C	N/A	

双时钟源
ModBus
接收超时中断
自动波特率
Tx/Rx管脚可配置调换

全双工异步通信
可编程过采样模式
可编程数据宽度
LIN 模式
IrDa 模式
Smartcard 模式
单线半双工模式

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分兼容 New features
LPUART	全兼容	N/A
CAN	N/A	N/A
		N/A
		全兼容 + Bug fixes
		不兼容 (no OTG on L1)
		N/A

全双工通信模式
可编程波特率
双时钟源
唤醒stop模式下的MCU
可编程数据宽度
RS-485发送器

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
USART	全兼容	部分兼容 New features
LPUART	全兼容	N/A
CAN	N/A	N/A
SAI	N/A	N/A
		全兼容 + Bug fixes
		不兼容 (no OTG on L1)
		N/A

CAN 2.0
通信率1Mbit/s
支持时间触发通信配置
三个发送邮箱
两个带三个状态的接收fifos

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
I2C	全兼容	不兼容 New features
SPI	部分兼容 New features no I2S (SAI)	部分兼容 New features no I2S (SAI)
		部分兼容
	N/A	兼容 Bug fixes
USB OTG FS	不兼容 (no OTG on L0)	不兼容 (no OTG on L1)
SWPMI	N/A	N/A

NEW:
USB OTG
附加检测协议(ADP)
电池充电检测(BCD)
链接电源管理(LPM)
独立VDDUSB

USB2.0 full-speed
可配置1~8个端点
支持同步传输
USB挂起恢复操作
USB连接检测

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
External memory interface	N/A	兼容 New features
Quad SPI	N/A	N/A
DFSDM	N/A	N/A
LCD	全兼容 New features	兼容 New features
AES	全兼容 New features	全兼容 New features
RNG	全兼容	N/A
Touch Sense Controller	全兼容	N/A

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
TIMERS	全兼容 + Enhancement	全兼容 + Enhancement
LP TIMER	全兼容	N/A
RTC	全兼容 + minor features	全兼容 + minor features
WWDG	全兼容	全兼容
IWDG	全兼容	兼容. + Window mode

全系列功能的兼容性

STM32L4 peripheral	From STM32L0	From STM32L1
ADC	不兼容	部分兼容
DAC	完全兼容	兼容
Comparators	部分兼容	不兼容
Operational amplifiers	N/A	不兼容
VREF Buffer	N/A	N/A

FIREWALL + 典型应用

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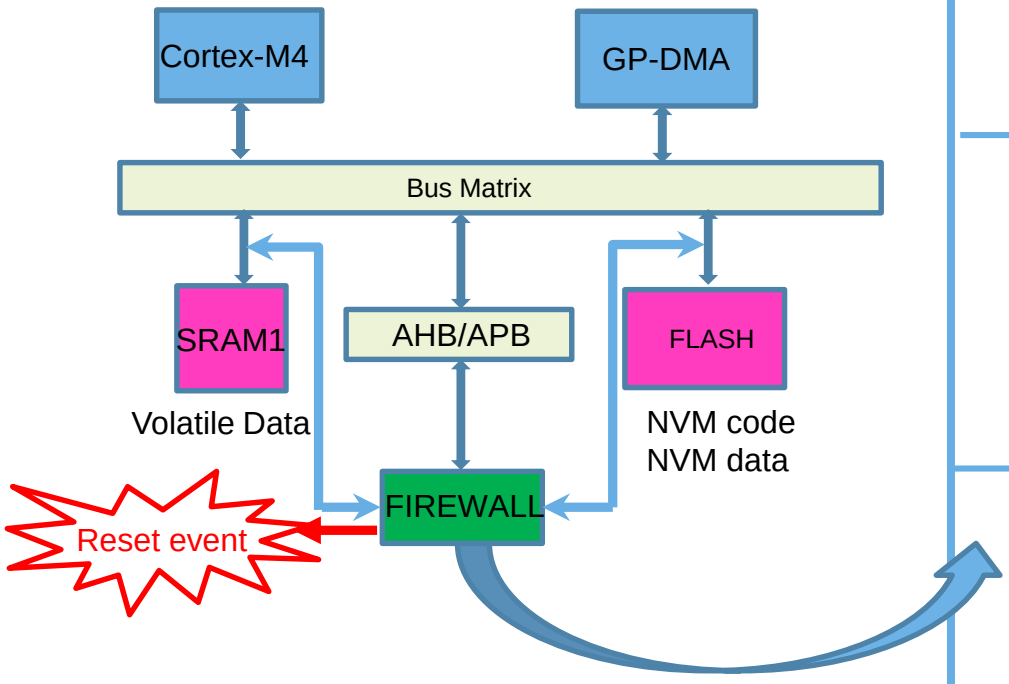
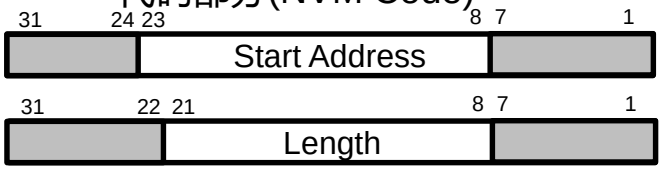
STM32 Firewall (FW)

- FIREWALL 用于保护指定区域的代码和数据(非易失性和易失性数据)

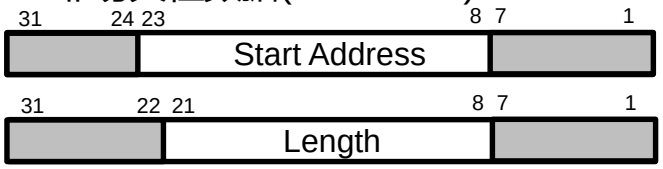


代码部分(NVM Code)



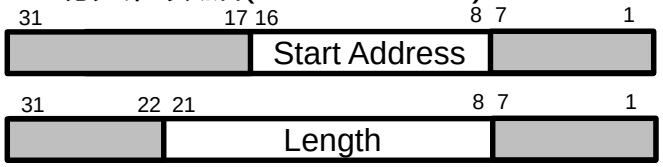
Protection : Code fetch

非易失性数据(NVM Data)

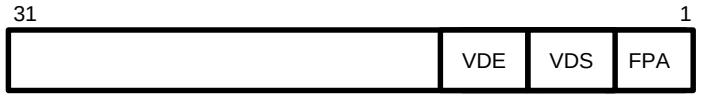


Protection : Data

易失性数据(SRAM1 Data)



保护: - 代码,如果在sram中执行
- 数据

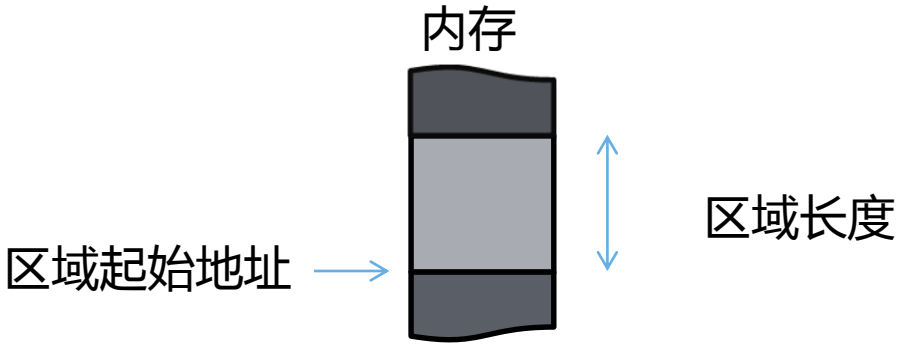


FW_CR

FPA : 预警位用于控制退出保护区代码
VDS : SRAM1 保护区域对于非保护区代码是共享的
VDE : SRAM1 是执行在易失性数据区域

STM32 FIREWALL

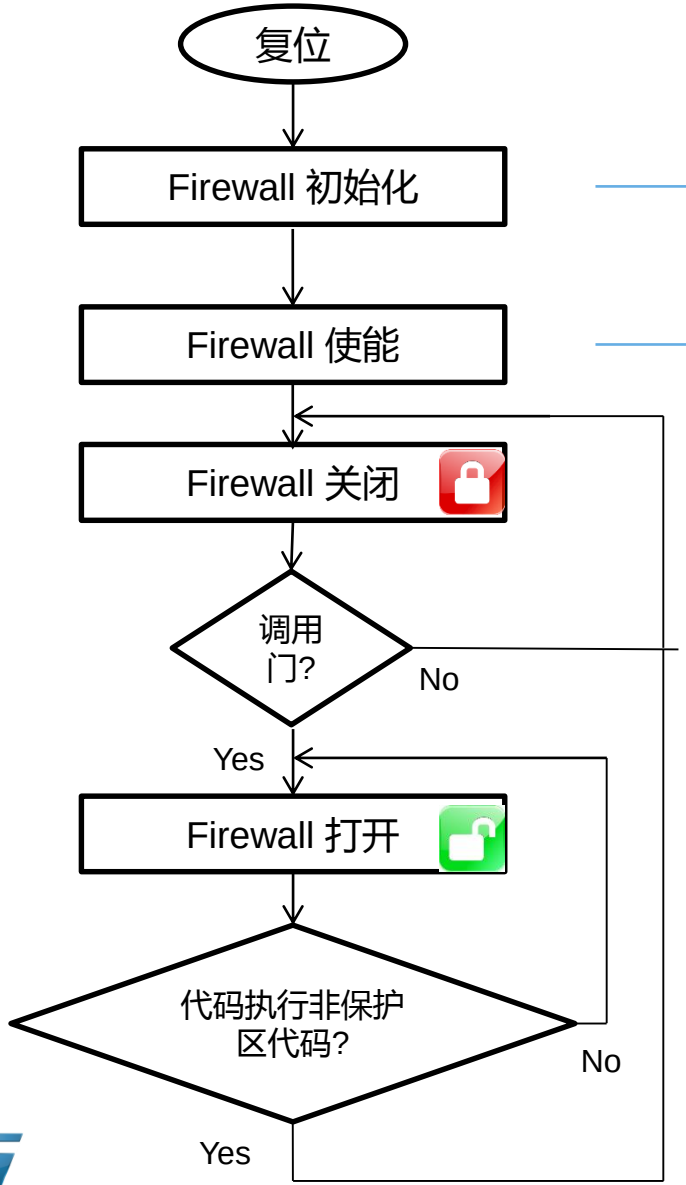
- 保护区域受到firewall的控制
  - The Firewall 包含三个区域, 每个区域都包含起始地址和区域长度两个寄存器.
    - 非易失性代码区域(Flash or EEPROM)
    - 非易失性数据区域(Flash or EEPROM)
    - 易失性数据区域 (RAM), 可以在上面执行代码或共享



- 在对FIREWALL初始化完成,并对FIREWALL 使能后,保护区域开始保护
  -> 在这后,所有的寄存器都被锁住直到下次复位

- 所有未经授权来自代码或者DMA的访问到保护区域,都会产生一个硬件复位.

STM32 Firewall 状态



通过FW的寄存器,配置所有保护区域的起始地址和长度

使能FIREWALL

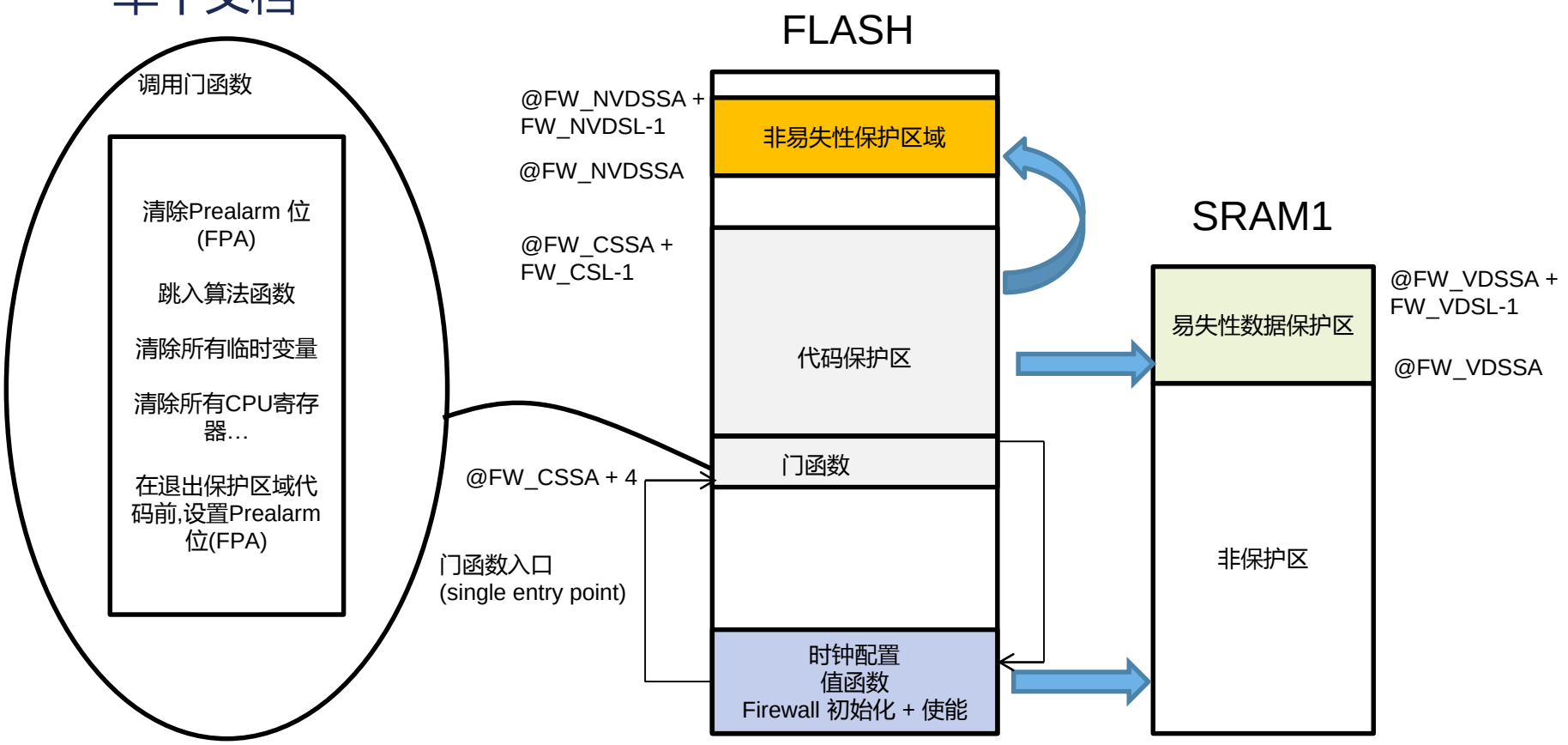
Call gate 区域 : 代码执行at @FW_CSSA + 4
或代码执行在@FW_NVDSSA + 4 如果SRAM1 定义为执行代码区域 (VDE =1 and VDS = 0)

代码执行跳出:

- @fetch ≤ @FW_CSSA or @fetch > @FW_CSSA + FW_CSL-1
- @fetch ≤ @FW_VDSSA or + @fetch > FW_VDSL-1 if VDE = 1 and VDS = 0

STM32 Firewall 典型应用1
客户研发全部FIREWALL

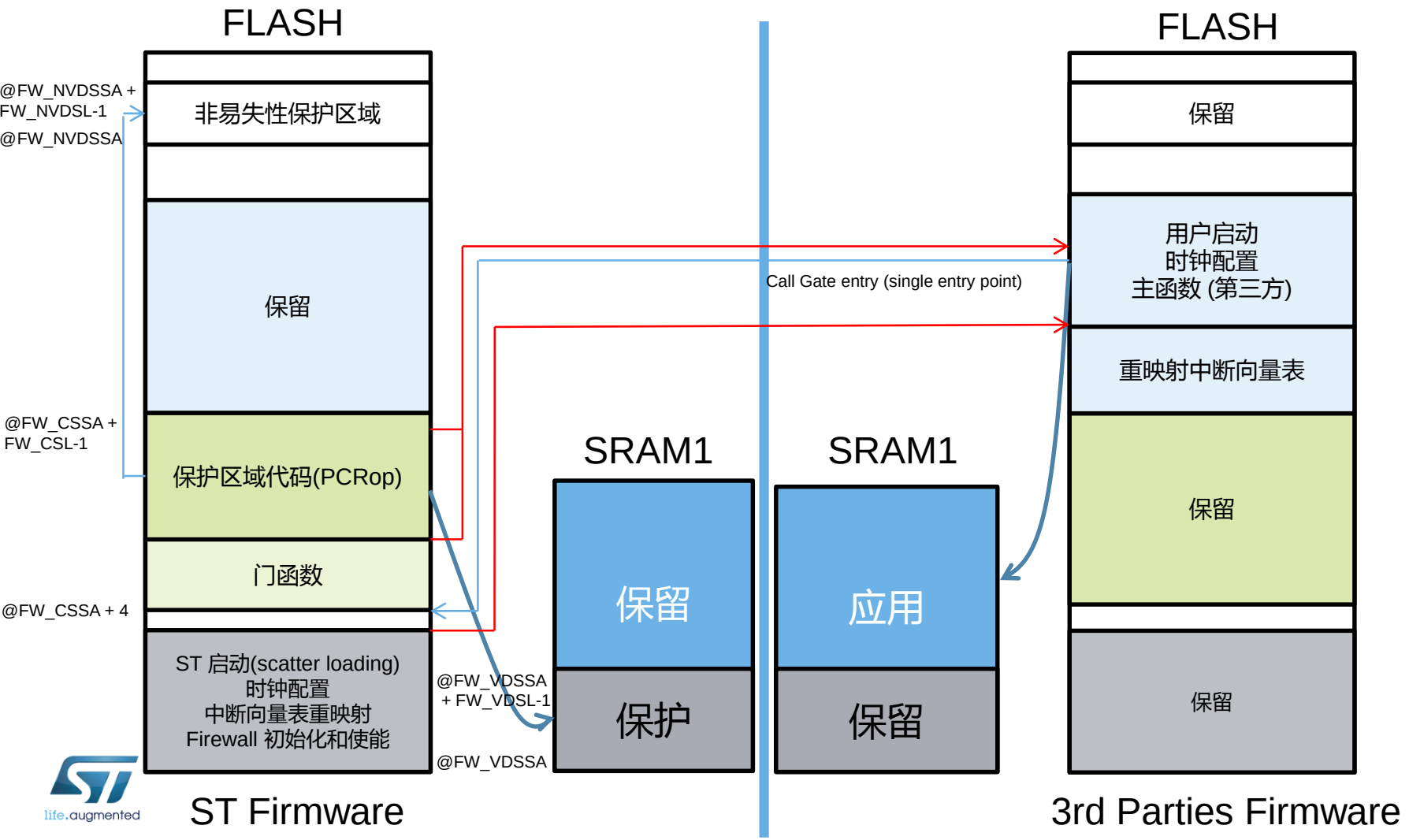
- 单个文档

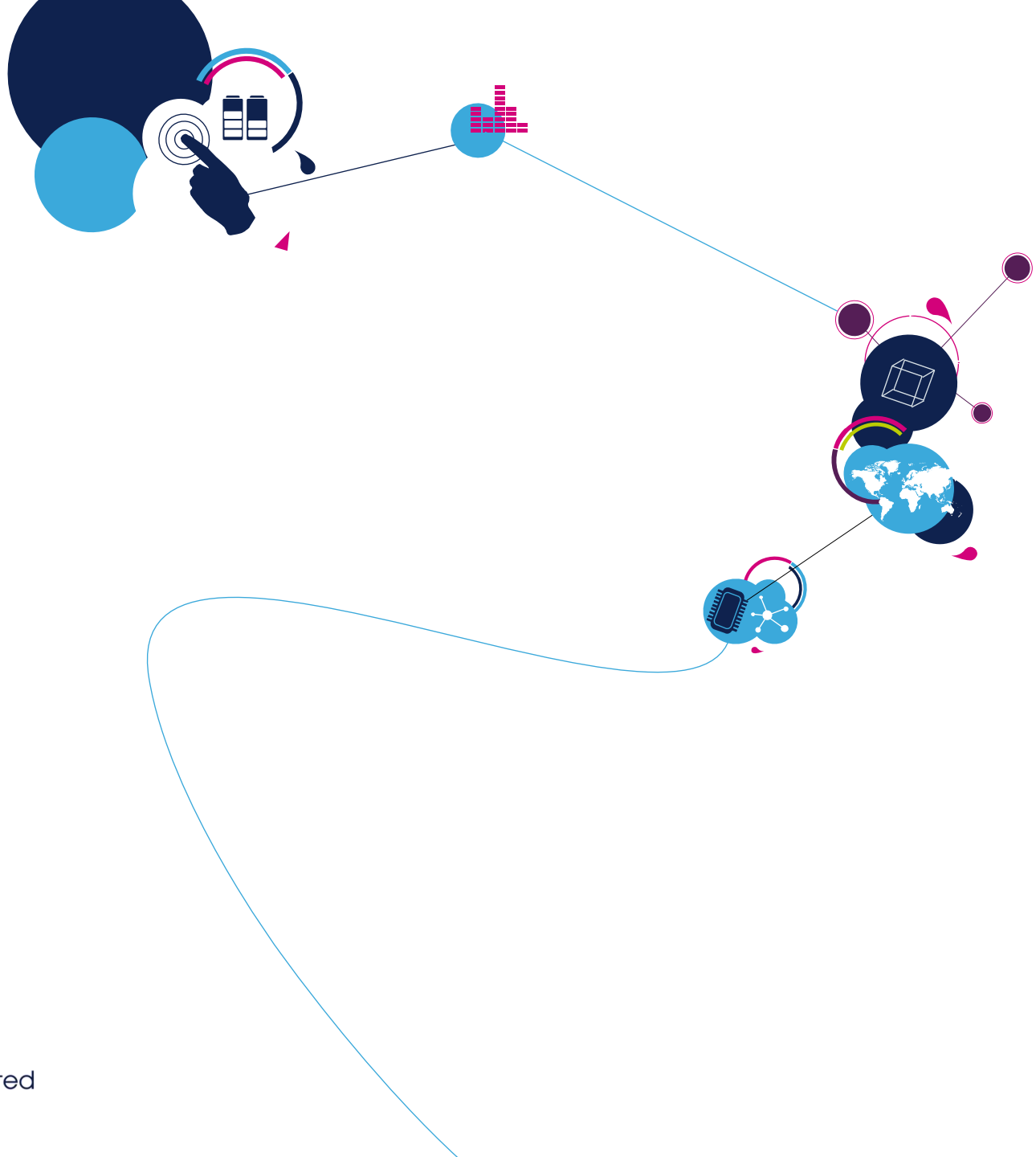


- Highest protection is Flash Level 2.
- PCRop protection may be set on the protected Code to avoid any read from a user code execution to dump it.
- In the call gate function, it could be secure to check at different places in the protected code that the Firewall enable bit is set and the Firewall registers configured as expected.

STM32 Firewall typical use case 2
Firmware 通过第三方研发

- 工程有多个文档: MIFARE® Classic





QuadSPI

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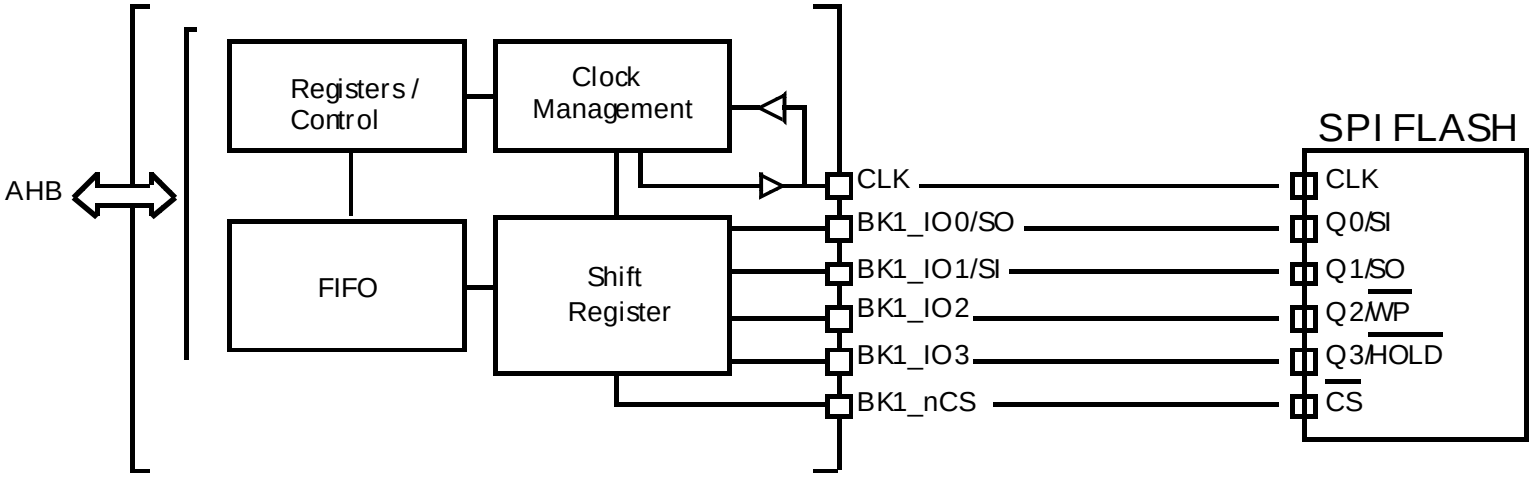
- **通讯接口：single/dual/quad SPI**
- **三种操作模式**
  - **间接**：全部的操作都是通过寄存器实现(经典 SPI)
  - **状态轮询**：周期性的查询FLASH的状态寄存器(中断)
  - **内存映射**：读操作类似于内部的FLASH



单内存模式

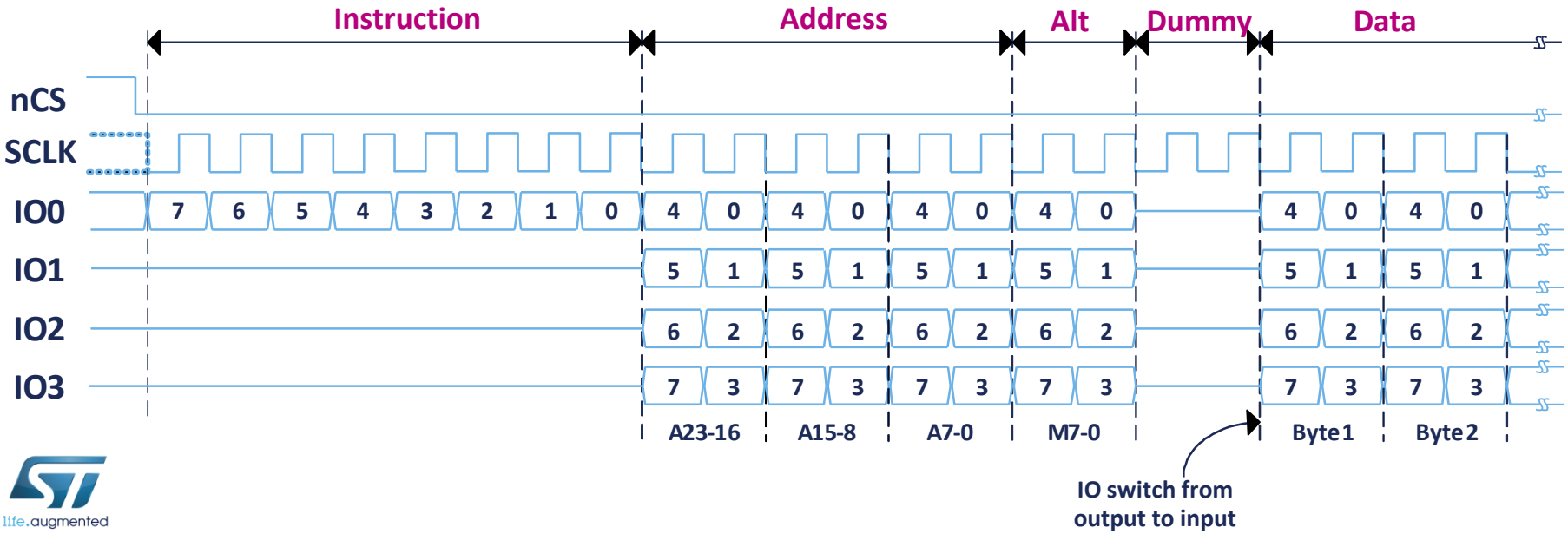
主要功能

- **三种功能模式**:
  - 间接
  - 状态轮训
  - 内存映射
- **优化操作**
  - 支持SDR 和 DDR
- **全部可编程**
  - 针对间接模式和存储器映射模式，完全可编程操作码
  - 针对间接模式和存储器映射模式，完全可编程帧格式
- **发射和接收都有完整的FIFO**
  - 允许8,16,32位数据访问
  - 间接模式有DMA模式
- **中断源:FIFO 门槛, 超时, 操作完成, 和操作错误**

帧格式

- **五个阶段的每个部分都可以配置**
  - 使能与否
  - 长度
  - 线数

- **例子**
  - 单线的指令部分
  - 地址, 备用字节 & 数据 都是4线
  - 2 个空指令周期



三种模式

- **间接模式**
  - 需要对寄存器一个个操作,类似传统SPI
  - 操作软件触发
- **状态轮询模式**
  - 存储最多四个字节,然后等待中断后检测匹配标志位
  - 操作硬件触发
- **内存映射模式**
  - FLASH视为内部FLASH,只是存在访问延时
  - 只能进行读操作
  - 无需寄存器操作

摘要

- **支持QuadSPI flash**
- **支持全编程和配置**
  - 支持市场上所有的QuadSPI flash
  - 支持新的指令,而不用硬件修改
- **特定的模式来轮询状态而不用 CPU**
- **由于内存映射模式,易于集成的现有firmware**

STM32 Digital Filter for Sigma Delta Modulators

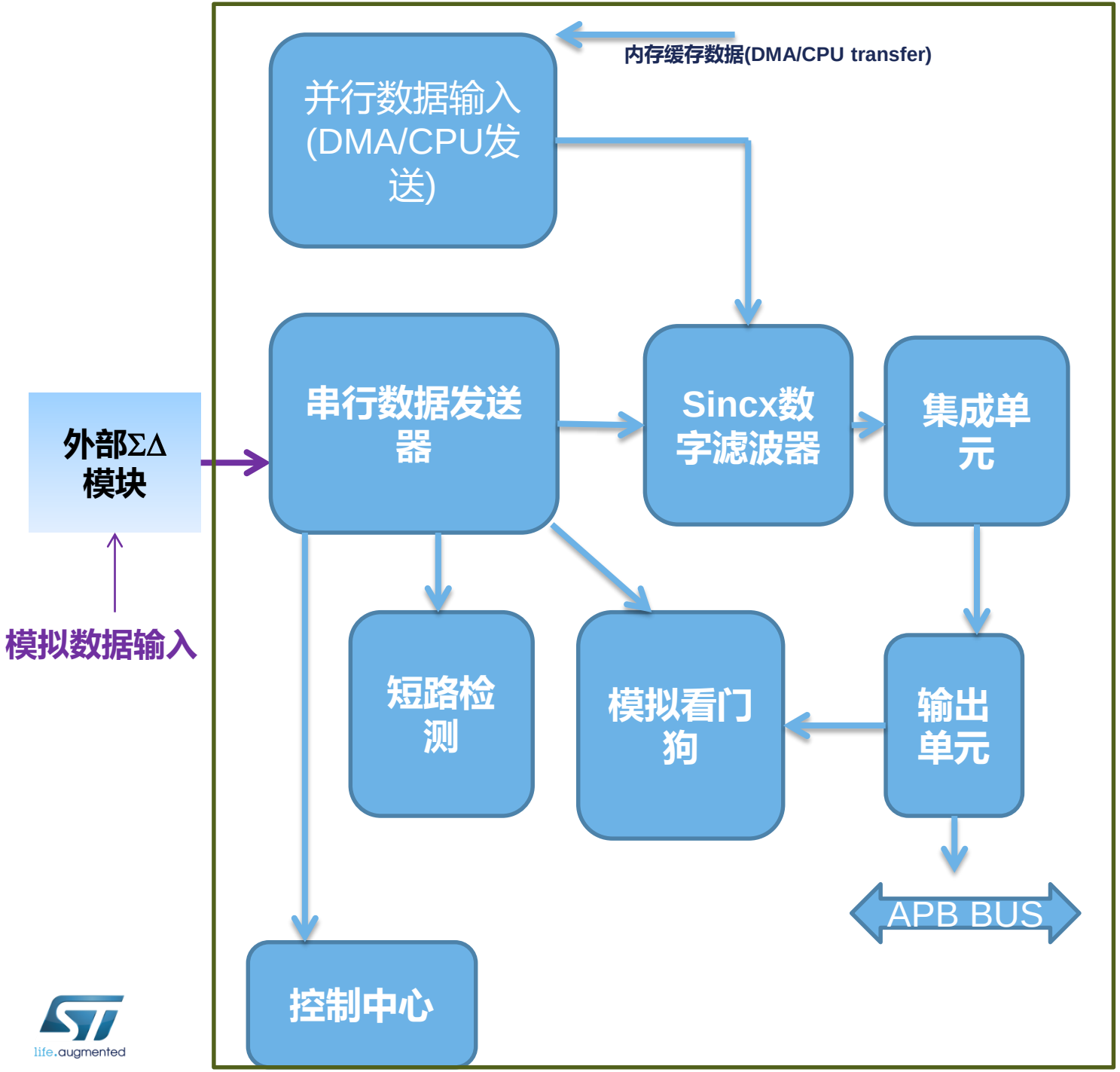
life.augmented

- **市场上外部的ΣΔ 模块:**
  - 这是一个外部单独的设备: ADC 通过sigma delta原理转换
  - 模拟输入 (通常是差分) 和数字输出
    - 精度: ~16-bit 分辨率
  - 提供快速的1位数据流的数字输出 => 串行接口
    - 高达 20MHz
  - 供应商广泛 (ST, TI, Analog Devices)

- **STM32 接口: DFSDM = Digital Filter for Sigma Delta Modulators**

  实现了完整的事后处理外部 ΣΔ 模块输出:
  - 从SD调制器接收数据流.(在不同的串行数据流)
  - 对数字流进行数字滤波(final 24-bit result)
  - 安全/应急功能

框架图



频段选择

- **注入通道**
  - 可以选择其中或全部通道
  - 扫描模式,全部选中的channel一个个轮流转换
  - 单个模式:只有一个通道转换
  - 触发转换,通过软件或硬件.(时间输出或者外部pin脚)
- **定时通道**
  - 只有一个channel被选中
  - 通过软件启动
  - 定时连续转换可以通过转换中断来被注入.

串行收发器

- **功能**
  - 接收和解码的原始串行流和提供给滤波器数据和时钟(最多有8路串行输入)
- **支持以下协议**
  - 单线曼切斯特编码模式
  - SPI:时钟和数据线
    - 时钟信号: 主端或从端
    - 配置选项:
      - 采样边缘, 时钟速度
      - 输入时钟频率测量(速率), 时钟存在检测
    - DFSDM 时钟输出: 可调节的两个时钟源
      - 系统时钟源(同步输入时钟)
      - 音频的PLL时钟源

并行收发器

- **功能**
  - 接收16位并行数据流从内部源到滤波器
  - 最多8路并行输入channel
- **内部数据源**
  - 内部ADC数据结果*(STM32L4x6没有)*
    - 最多支持8路内部ADCs数据连接
    - 数据转移从ADC到专用的十六位输入寄存器
  - RAM数据 (DMA/CPU transfers from memory)
- **使用**
  - ADC数据处理
  - 收集数据的后期处理

Sincx的数据滤波器

- **数据滤波器执行对输入流的滤波**
- **Sinc 滤波命令可以如下配置**
  - $Sinc^1$, $Sinc^2$, $Sinc^3$, $Sinc^4$, $Sinc^5$
  - FastSinc
  - 没有滤波(在整合阶段的位流发送)
- **编程sincx的过采样率**
  - 从1到1024的样品过滤器
- **最大31位的输出滤波分辨率**
    - (e.g.: $Sinc^3$ with oversampling by 256)

集成单元

- 集成阶段执行额外信号处理-从数字滤波器的数据平均(求和N个样品)
- 集成长度(N)可以被配置
  - 从1到256个样品
  - 一旦集成完成最后的结果发送到data bus.积分器就会复位
- 积分器可用在运行中reset
  - 硬件:触发器从外部触发或者timer
  - 通过过滤器的配置修改(顺序,过采样率)

输出单元

- **后期处理功能**
  - 偏移补偿
    - 存储器偏移数据的减法(用户应手动校准偏移)
  - 可编程的右移的数据格式
    - 最大暑输出24-bit
    - 需要移位依赖于滤波器和积分器的设置
  - 在被写入输出寄存器之前,最后的结果的样品处理
- **附加功能**
  - 最小/最大极端检测:允许监控动态转换在延长的时间周期
  - 模拟看门狗(为了观察最后的数据边界溜出)

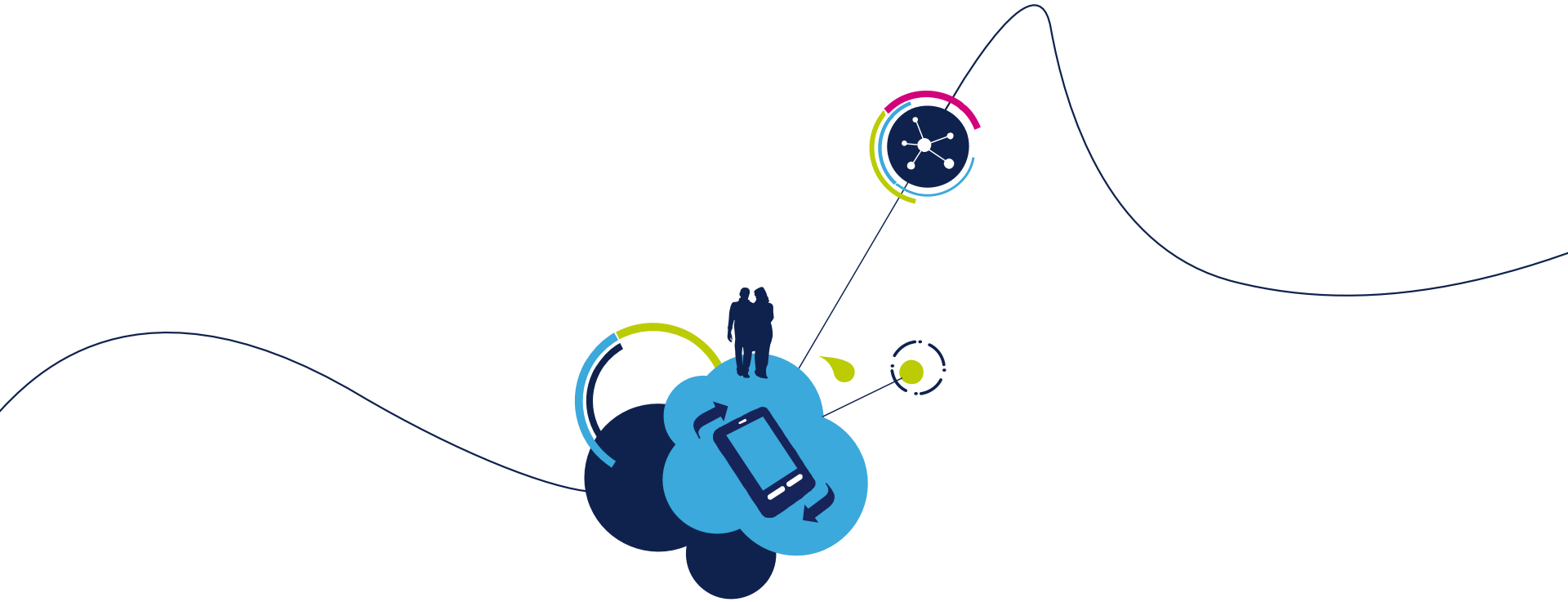
- **有几个步骤关于关键的应用状态检测:**
  - 模拟的看门狗
    - 速度和边界分辨率设置
  - 短路检测
    - 快速检测临界状态
  - 中断信号产生
    - 模拟看门狗和短路检测输出都可以产生一个硬件中断
    - 由硬件对临界情形作出反应

模拟看门狗

- **如果数值超出界限,就会产生中断信号**
  - 单独对高和低的通道检测
- **该信号可以采取于:**
  - 最终的输出数据
    - 速度较慢,但是精度高(最后输出分辨率可以达到24bit)
  - 从原来连续数据流输入,通过配置自身的滤波器(对每个输入通道):
    - 更快的响应,带有可配置参数(独立于主滤波器而独立操作)
    - 拥有过滤器:
      - $Sinc^1$, $Sinc^2$, $Sinc^3$, FastSinc filter
      - Oversampling ratio: 1-32
- **看门狗的数量:**
  - 模拟看门狗有8个串行输出口(8 channels)
    - 8 路通道都可以各自输出看门狗数据寄存器
  - 但限制入口的数量
    - 一个主数字滤波器一个门限=> 4 个门限
    - 主滤波器模拟门限分配到一个或多个输入通道

短路检测

- **如果数值超出边界,就会产生中断信号**
- **边界定义为在输入频段接收连续的0和1数据流**
  - 因为ΣΔ 调制器输出数据流提供 1's 和 0's ,还有范围超出所有 1's 或 所有 0's (outside +/- range)
  - 设置阈值范围: 1 – 256 连续计数
- **所述信号取自在每个输入通道流**
  - 计数器计数连续1's 或 0's ,如果达到通道的门限,则产生事件
  - 所有输入通道都有效(8个通道)
  - 相对于主数字滤波器可以独立操作



谢谢

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